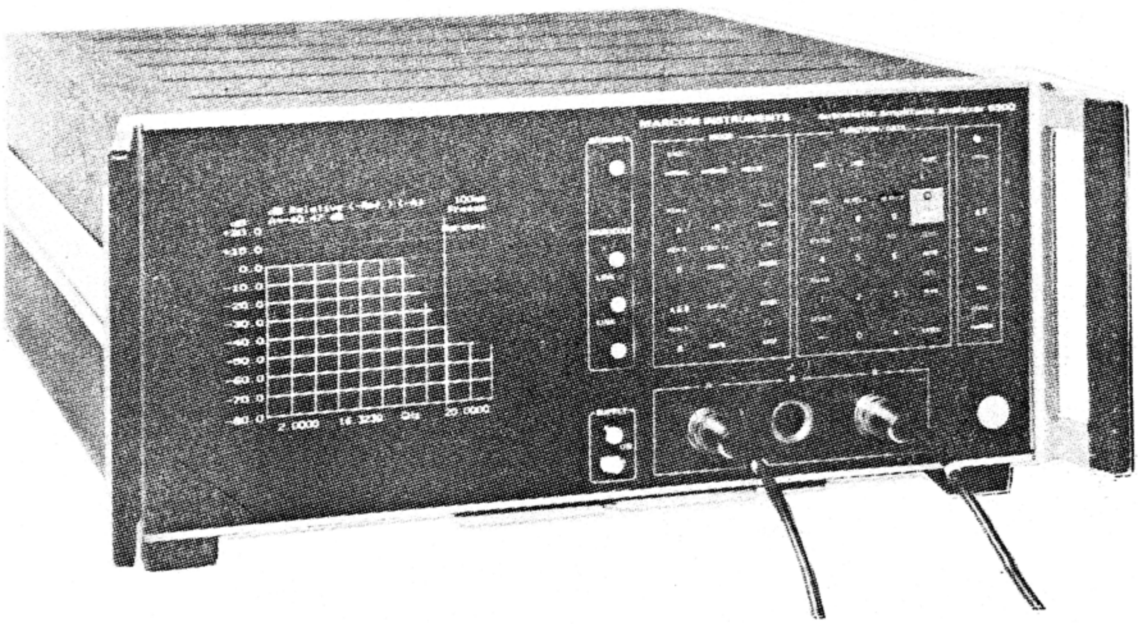
Operating Manual
H 6500
Vol.1

AUTOMATIC AMPLITUDE ANALYZER
6500



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PREFACE

WARNINGS, CAUTIONS and NOTES

These terms have specific meanings in this manual:

WARNINGS contain information to prevent personal injury.
CAUTIONS contain information to prevent damage to the equipment.
Notes contain important general information.

HAZARD SYMBOLS

The meaning of hazard symbols appearing on the equipment is as follows:-

Symbol	Nature of hazard	Reference in manual
⚠	Dangerous voltages	Page iv
⚠	Static sensitive components	Page v

MANUAL AMENDMENT STATUS

Each page in this manual bears the date of its original issue or, if it has been amended, the date and status number of the amendment. Any changes subsequent to the latest amendment status are included on Manual Change sheets coded C1, C2 etc. at the front of the manual.

CONTENTS

ASSOCIATED PUBLICATIONS

Programming Manual, H 6500 Vol. 1A (for GPIB operation)
Service Manual, H 6500 Vol. 2
Programmable Sweep Generator 6310 (2 - 20 GHz) Op. Manual, H 6310 Vol. 1
Programmable Sweep Generator 6311 (0.01 - 20 GHz) Op. Manual, H 6311 Vol. 1
6500/6310 Automatic Analysis System: Software Support Pack Manual, H 6500SSP

OPERATING PRECAUTIONS

This product has been designed and tested in accordance with IEC Publication 348 - 'Safety Requirements for Electronic Measuring Apparatus'. To keep it in a safe condition and avoid risk of injury, the following precautions should be observed.

WARNING - ELECTRICAL HAZARDS

AC supply voltage. This equipment conforms with IEC Safety Class 1, meaning that it is provided with a protective earthing lead. To maintain this protection the mains supply lead must always be connected to the source of supply via a socket with an earthing contact. Make sure that the earth protection is not interrupted if the supply is connected through an extension lead or an auto-transformer.

Before fitting a non-soldered plug to the mains lead cut off the tinned end of the wires, otherwise cold flowing of the solder could cause intermittent contact.

Do not use the equipment if it is likely that its protection has been impaired as a result of damage.

Primary fuses. Note that there is a supply fuse in both the live and neutral wires of the internal supply lead. If only one of these fuses should rupture, certain parts of the equipment could remain at mains potential.

To provide protection against breakdown of the internal supply lead, its connectors or filter (if fitted); a fuse should also be used in the live wire of the external supply lead (e.g. fitted into the mains plug). The fuse should have a continuous rating not exceeding 6A.

Make sure that only fuses with the required rated current and of the specified type are used for replacement. Do not short-circuit the fuse holder or use mended fuses.

Secondary fuses. Each secondary winding of transformer T1 (with the exception of +5 V and +12 V supply lines, which are adequately protected by the primary fuses F1 and F2) is fused with a 250 mA, A-T (250 milliamp time lag) fuse to provide added safety. These are situated on the secodary tag board within the instrument and can be accessed by removing the lower cover. See Service Manual.

Removal of covers. Disconnect the supply before removing the covers so as to avoid the risk of exposing high voltage parts. If any internal adjustment or servicing has to be carried out with the supply on, it must only be performed by a skilled person who is aware of the hazard involved.

Remember that capacitors inside the equipment, including any supply filter capacitors, may still be charged after disconnection of the supply. Those connected to high voltage points should be discharged before carrying out work inside the equipment. This applies particularly to the EHT circuit for the cathode ray tube which must be discharged by repeatedly shorting the final anode lead to chassis, or by using a bleed resistor. The residual charge on the CRT itself should also be removed by shorting the anode connector to chassis.

WARNING - OTHER HAZARDS

Parts of this equipment are made from metal pressings, therefore it should be handled with due care to avoid the risk of cuts or scratches.

Some of the components used in this equipment may include resins and other materials which give off toxic fumes if incinerated. Take appropriate precautions, therefore, in the disposal of these items.

Cathode ray tube. Be careful when exposing or handling the cathode ray tube, because of the risk of implosion and consequent scattering of glass fragments. Handling should only be carried out by experienced personnel and the use of a safety mask and gloves is recommended. A defective tube should be disposed of in a safe manner by an authorized waste contractor.

CAUTION - STATIC SENSITIVE COMPONENTS

This equipment contains static sensitive components which may be damaged by handling - refer to the service manual for handling precautions.

Chapter 1

GENERAL INFORMATION

FEATURES

The 6500 Automatic Amplitude Analyzer provides accurate scalar measurements quickly and efficiently. All relevant data is presented on the CRT display and the user is able to control any external sweeper utilizing an external ramp. When operated with Marconi Instruments 6300 seies Programable Sweep Generators, a complete scalar analysis system is formed, with intelligent interaction between the instruments to enhance system performance. Details of system operation are given in the appropriate 6300 series manual.

Microprocessor control allows a variety of measurements to be made simply and accurately. Three input channels A, B and R are available. Channels A & B are used as measurement channels and channel R as a reference, when required. The response on the channel R may be subtracted from channels A and/or B, enabling measurements to be made independently of sweeper frequency responses and level variations. Three memories are provided to allow normalization or comparisions to be made between current and stored responses.

Measurements over a frequency range up to 126 GHz are possible depending on the detectors used. The detectors 6511, 6512 6513 and 6514 allow measurements over the range 10 MHz to 40 GHz to be made.

The variable "brightline" allows spot level measurements to be made anywhere within the frequency sweep range. The brightline level measurement and the corresponding frequency are displayed at the top and bottom of the display to 0.01 dB and 10 MHz (max.) resolution.

Display sensitivity (RANGE) can be set from 0.1 to 10.9 dB(m) per division and the DATUM in the range ±99.9 dB(m); both these parameters can be set independently on each channel. Alternatively, the AUTO facility will automatically select the best DATUM and RANGE to fit the trace(s) on the screen, relieving the user of the task of setting them manually. In addition, the required sweep width can be set anywhere within the sweepers range to a resolution of 10 MHz.

A facility for checking responses to specification is provided by the limit facility. HIGH and LOW limits may a be individually entered for the ´A´ and ´B´ channels. If any limit is exceeded during a sweep a warning message is generated on the alphanumeric display. Up to 9 sets of display parameters and limits may be stored and recalled thus allowing fast testing of devices to different specifications in different frequency bands.

The sweep can be stopped to permit photography or plotting. The PLOT facility uses an X-Y plotter to plot the displayed traces and appropriate amplitude and frequency scaling.

All the 6500 keyboard functions can also be programmed by the general purpose interface bus (GPIB) if the interface is fitted. The interface is available in the 6500-001 version of the instrument, or as an accessory: 3964-650. This option also allows many facilites additional to those available from the front panel, which optimise the 6500's use in an automatic test system.

Display Characteristics

The front panel provides an integral green phosphor CRT for display of all measurement information. The main display components are illustrated in Fig. 1-1 below.

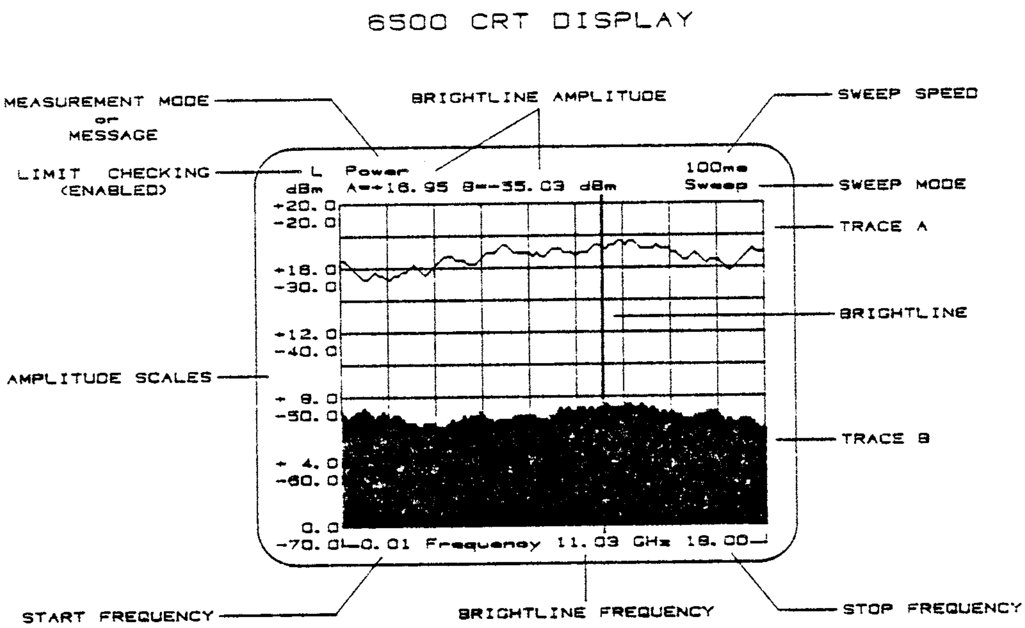


Fig.1-1 Display components

Alphanumerics The alphanumeric display provides a 40 x 25 character format for display of measurement parameters, user promts and other messages. The top line of the display is reserved for the title of the measurement, e.g.

Power
dB Relative
Gain/Loss (-Ref) (-A,R)

and also for displaying the selected nominal sweep speed. If the GPIB interface is fitted, this line can be replaced with any title up to 28 characters long.

Graticule The graticule lines on the frequency (X) axis are placed by the microprocessor at calculated intervals in order to provide standard frequency divisions in multiples of 1.2 or 5. These will vary depending on the actual sweep width selected. On sweep widths of 100 MHz or less these are not produced. On the amplitude (Y) axis there are ten fixed divisions which can be set to cover from 0.1 to 10.9 dB(m) per division.

Channel display Two line display memories (A,B) allow channels A and B to be displayed singly or simultaneously. When the reference channel (channel R) is displayed, its display information is held in display memory A. Each display memory contains measurement information for 422 horizontal measurement points, with a vertical resolution of 256 points. (Note that this apparently limited vertical resolution applies to to the characteristics of the displayed trace only - power resolution to 0.01 dB will be provided by the digital readout whatever the power scale). Each channel can be displayed in 'line' or 'histogram' form, although the R channel will be displayed in the same form as the A channel. When a sweep is started, the relevant channels will be switched on and cleared. On all subsequent sweeps each point will be updated as the measurement is made, thus providing a flicker-free display.

Brightline. The Brightline is a single moveable vertical line, which can be placed anywhere within the graticule. It is used for spot measurement purposes and the information relating to the amplitudes and its position on the frequency axis is displayed above and below the graticule respectively - see Fig. 1-1.

Up to 8 markers can be placed on the screen using the Brightline. These are fixed in position and are for visual reference. When PLOT facility is enabled these appear as tick marks on the hard copy.

SPECIFICATION

Characteristic	Performance
Frequency range:	0-126 GHz (dependent on detector).
Dynamic range (All channels)	
Normal mode:	66 dB (+16 dBm to -50 dBm).
Average mode:	71 dB (+16 dBm to -55 dBm).
Resolution (Brightline)	
Frequency:	Digital readout to 10 MHz.
Amplitude:	Digital readout to 0.01 dB(m)
Frequency Linearity:	Dependent on linearity of sweeper, See Ramp output linearity.
Markers:	Up to 8 on-screen markers with 10 MHz resolution.
Front panel selectable parameters	
Range:	0.1 to 10.9 dB(m) division; 0.1 dB(m) increments.
Datum:	±99.9 dB(m); 0.1 dB(m) increments. Above parameters individually selectable on A,B and R channels.
High/Low Limits:	±99.99 dB(m) individually selectable on A and B channels.
F1,F2 (Sweep range):	Selectable in range 0-126 GHz; (10 MHz resolution).
Start,Stop (Selected range):	Selectable within range F1-F2; (10 MHz resolution).
ΔF:	Selectable symmetrically within range F1-F2; Centre Frequency is Brightline position. (10 MHz Resolution)
Display format:	Line or histogram independently on A, B channels.
Sweep speed:	70 ms to 20 s nominal (10 alternative speeds).

Characteristics	Performance
X-Y plotter functions:	Plot all. Set pen bottom left. Set pen top right. Set pen to origin. Draw axes. Label axes. Plot. Set pen lift. Set plot speed (9 alternatives). Set live Y.
Digital plotter functions:	Available if GPIB interface fitted
Ramp output	
Output 1 (Fixed range)	
Range:	0 - 10 V ±10 mV.
Linearity:	±5 mV.
Resolution:	4096 points.
Output 2 (Variable)	
Range:	Adjustable from 1 - 20 V (approx.) using coarse and fine rear panel controls.
Offset:	Bottom of range = 0 V ±10% of range (above).
Linearity:	±0.25%
Resolution:	4096 points.
Plotter output	
X output:	See Ramp output 1: BNC socket.
Y output:	0 - 10 V ±50 MV: BNC socket.
Z output:	Open collector drive: BNC socket selectable high/low impedance for pen up/down.
Channel memories:	At any time when valid data is available on the screen, the trace may be stored in any of the three memories. New data may be averaged with data already present. When invoked:- A memory is subtracted from A trace. B memory is subtracted from B trace. R memory is subtracted from A and/or B trace, as selected. Recall is available on all memories.

Characteristics	Performance
CRT	
Dimensions:	105 mm x 135 mm used screen area.
Phosphor:	Green.
Power requirements	
Voltage:	AC supply. Voltage ranges (switchable) 105 - 120 V or 210 - 250 V.
Frequency:	50 to 60 Hz.
Consumption:	120 VA maximum.
Safety:	Meets IEC 348.
Radio Frequency interference:	Conforms with he requirements of EEC Directive 76/889 as to limits of RF interference.
Temperature range	
Operational:	0 - 50 °C.
Full specification:	10° - 35 °C.
Conditions of storage and transport	
Temperature:	-40 °C to +70 °C.
Humidity:	95 % relative at 35 °C.
Dimensions and weight (approximately)	With handles and feet.
Height:	192 mm (7.5 in).
Width:	427 mm (16.8 in).
Depth:	533 mm (21.2 in).
Weight:	15.7 kg (34.5 lb).
Remote programming	A GPIB interface compatible with IEEE-1978 is available either fitted (in the 6500-001) or as an optional accessory (3964-650). Another accessory (46883-408K) is available to allow conversion to IEC 625 format.

VERSIONS AND ACCESSORIES

Versions	Part no.
Automatic amplitude analyzer	6500
Automatic amplitude analyzer with GPIB	6500-001
Automatic amplitude analyzer with GPIB (400 Hz operation)	6500-002

Supplied accessories

AC supply lead	23424-158H
Operating manual	46881-557V
Programming manual (supplied with 6500-001 and -002)	46881-558S

Detectors

0.01 - 20 GHz, Type N male connector	6511
0.01 - 20 GHz, Type APC-7 connector	6512
0.01 - 26.5 GHz, Type MPC 3.5 connector	6513
26.5 - 40 GHz, Flange face UG 399/U	6514
0.01 - 18 GHz Wiltron Autotester 560-97A 50, Type APC-7 connector, complete with adapter cable	59999-151W
0.01 - 26.5 GHz Wiltron Autotester 560-98 S50, Type APC-3.5 connector, complete with adapter cable	59999-152D

Optional accessories

Cables:	6510 Series detector extender cable, 5 m	3964-325
	Detector adapter cable (BNC), 2 m	3964-294
	6500-SMA cable, 2 m	3964-326
	GPIB cable, 1 m	43129-189U
	Interface cable to HP 8620C	3964-003
	BNC-BNC cable, 1.5 m	43126-012S
	N(m)-N(m) cable, 1 m	2200-277
Measurement accessories:	High directivity coupler, 1-18 GHz	2200-332
	Power divider, 2-18 GHz	2200-335
	Microwave bridge set, 2-18 GHz, 36 dB directivity	2200-327
	Waveguide coupler, 8.2 to 12.4 GHz, 10 dB	6030A/10
	Waveguide to N type transformer, 12.4 to 18 GHz	6237/1
	Waveguide to N type transformer, 8 to 12.4 GHz	6237/3
Mechanical accessories:	Camera mount	3964-239
	Camera hood	46883-267B
	Rack mounting kit, 19 in.	3964-400
Service aids:	Service manual	46881-559Y
	Field-replaceable detector modules for 6511 and 6512	2716-006
GPIB interface		3964-650
Programming manual		46881-558S

Software support packages (SSPs)	Part no.
3.5 inch disc for use on external disc drive	3964-732
5.25 inch disc for use on 9826 and 9836 with internal disc drive	3964-733
Both SSPs are supplied with a comprehensive user manual:	46881-592V

ASSOCIATED EQUIPMENT

Programmable Sweep Generator, 2 - 20 GHz	6310
Programmable Sweep Generator, 0.01 - 20 GHz	6311

6500-500 SCALAR NETWORK ANALYZER SYSTEMS

All systems include:

Automatic Amplitude Analyzer (with GPIB)	6500-001
GPIB Lead Assembly	43129-189U
BNC Connection Cable (Qty. 2)	43126-012S
Precision Adapter N(m) - N(m)	59999-161R
Earth connection kit	3964-334

The other components of the systems are detailed below:

System	6310	6311	6511	6512	59999-151W
6500-501	1		3		
6500-511	1			3	
6500-541	1		1	2	
6500-551	1		2	1	
6500-521		1	3		
6500-522		1	2		1
6500-531		1		3	
6500-532		1		2	1
6500-561		1	1	2	
6500-562		1	1	1	1
6500-571		1	1	1	

DETECTOR SPECIFICATIONS

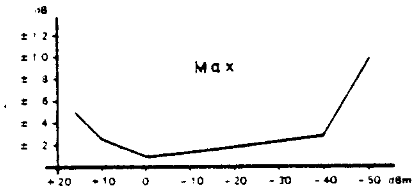
Performance specifications for detectors at present available are given below. Additional information will be available as the range of detectors is expanded to suit user requirements.

6511 Detector

Frequency range : 0.01 to 20 GHz.

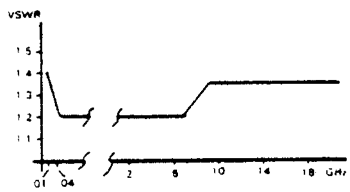
Dynamic range : -55 to +16 dBm.

Power accuracy at 50 MHz at 23°C ±4°C (excluding errors due to Return loss, Flatness and Source harmonics).



Maximum input power : +26 dBm average, +30 dBm peak.

VSWR :



Detector flatness, -10 dBm input power: ±0.5 dB from 0.01 to 18 GHz
+0.5 dB, -1.0 dB from 18 to 20 GHz

Connector : Precision type N.

6512 Detector

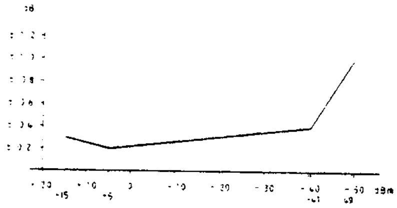
The 6512 differs from the 6511 only in that it has an APC-7 connector.

6513 Detector

Frequency range : 0.01 to 26.5 GHz

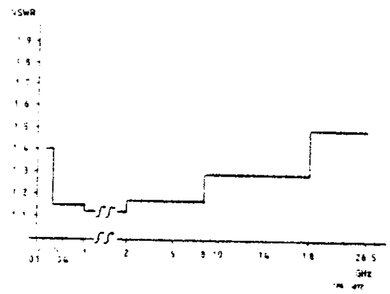
Dynamic range : -50 to +16 dBm

Power accuracy at 50 MHz and 23°C ∓4°C (excluding errors due to Return loss, Flatness and Source harmonics) :



Maximum input power : +26 dBm average, +30 dBm peak.

VSWR :

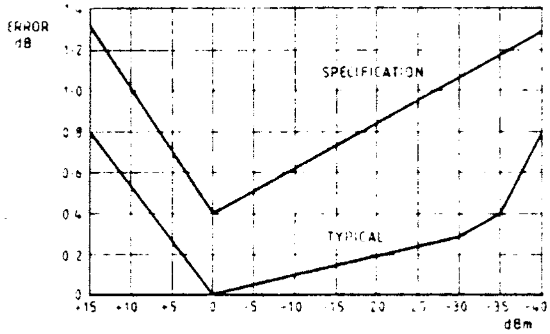


Detector flatness, -10 dBm input power: ±0.5 dB from 0.01 to 18 GHz
±1.0 dB from 18 to 26.5 GHz

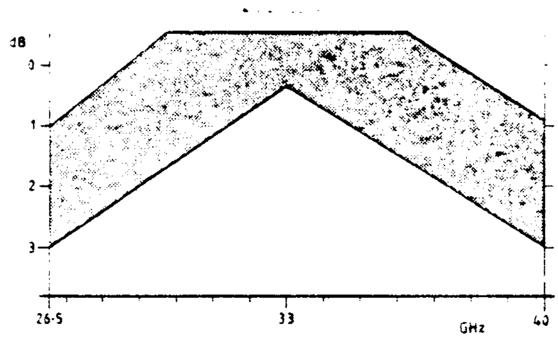
Connector: MPC 3.5 (m). Mates non-destructively with SMA and similar connectors.

6514 Detector

Frequency range :	26.5 to 40 GHz.
Dynamic range :	-45 to +10 dBm, usable to +16 dBm.
Power accuracy at 33 GHz at 21°C ±2°C : (including errors due to VSWR, flatness and source harmonics.)	±0.4 dB at 0 dBm.



Maximum input power	+20 dBm average, +23 dBm peak.
VSWR :	2.5:1.
Frequency response :	±0.3 dB at 33 GHz (-1 to -3 dB at band edges).



LIMITS OF FREQUENCY RESPONSE (MEASURED AT -10dBm)

Detector tracking :	Included in frequency response diagram shown above.
Operating temperature :	5°C to 40°C.(Do not use below dew point).
Input connector :	WG22 UG599/U.
Output connector :	Cable assembly to mate with 6500 input multiway.
Dimensions and weight :	Detector and waveguide extension. Length : 119 mm. Width : 25 mm. Height : 21 mm. Weight : 235 g.

Chapter 2

INSTALLATION

UNPACKING AND REPACKING

Retain the packing materials and the packing instruction note (if included) in case it is necessary to reship the instrument.

If the instrument is to be returned for servicing attach a label indicating the service required, type or model number (on rear label), serial number and your return address. Pack the instrument in accordance with the general instructions below or with the more detailed information in the packing instruction note.

(1) Place a pad in the bottom of the container.

(2) Place pads in the front and rear ends of the container with the plywood load spreader(s) facing inwards.

(3) Put the polythene cover over the instrument and place it in the container with the front handles and rear projections (where applicable) against the plywood load spreaders.

(4) Place pads in the two sides of the container with cushioning facing inwards.

(5) Place the top pad in position.

(6) Wrap the container in waterproof paper and secure with adhesive tape.

(7) Mark the package FRAGILE to encourage careful handling.

Note ...

If the original container or materials are not available, use a strong double-wall carton packed with a 7 to 10 cm layer of shock absorbing material around all sides of the instrument to hold it firmly. Protect the front panel controls with a plywood or cardboard load spreader; if the rear panel has guard plates or other projections a rear load spreader is also advisable.

MOUNTING ARRANGEMENTS

Excessive temperatures may affect the instrument's performance; therefore the plastic cover, if supplied, should be completely removed. Ensure that the fan air vent and other ventilation holes are not obstructed otherwise the maximum temperature specification is reduced resulting in imperfect operation. Avoid standing the instrument or associated detectors in the vicinity of large transformers or other possible magnetic fields or where X rays are present. If the source of such fields cannot be isolated Mumetal shields should be used to provide the necessary screening.

CONNECTING TO SUPPLY

Before connecting the instrument to the AC supply check the position of the voltage selector with. The range selected can be seen on the side of the switch protection plate situated on the rear panel.

The instrument is normally dispatched selected to the 210-250 V range. To select the 105-120 V range remove the protection plate, switch ranges and change the value of the AC supply fuses to that shown below, reverse ad refit the protection plate.

115 V range 1.25 A-T (1.25 amp time lag)
230 V range 600 mA -T (600 mA time lag)

Fuses are 20 mm x 5 mm cartridge type.

The supplied AC supply cable is fitted at one end with a female plug which mates with the AC connector at the rear of the instrument. When fitting a supply plug ensure that conductors are connected as follows:

Earth	-	Green/Yellow
Neutral	-	Blue
Live	-	Brown

Any interruption of the earth conductor is liable to make the equipment dangerous.

When attaching the mains lead to a non-soldered plug it is recommended that the tinned ends of the lead are first cut off owing to the danger of cold flow resulting in intermittent connections.

SAFETY TESTING

Where safety tests on the mains input circuit are required, the following procedures can be applied. These comply with BS 4743 and IEC Publication 348. Tests are to be carried out as follows and in the order given, under ambient conditions, to ensure that mains input circuit components and wiring (including earthing) are safe.

(1) Earth lead continuity test from any part of the metal frame to the bared end of the flexible lead for the earth pin of the user's mains plug. Preferably a heavy current (about 25 A) should be applied for not more than 5 seconds.

Test limit: not greater than 0.5 ohm.

(2) 500 V DC insulation test from the mains circuit to earth.

Test limit: not less than 2 M ohm.

GPIB INTERFACE (3964-650)

The GPIB interface is an optional accessory and can easily be fitted by the user, details are given in the Programming manual, Vol. 1A.

RACK MOUNTING

The instrument may be mounted in a standard 19 inch rack using the kit Part No. 3964-400 available as an optional accessory. Fitting instructions are as follows:-

(1) Disconnect the mains supply.

(2) Remove both top and bottom outer covers, detach and discard front and rear feet on bottom cover.

(3) Fit rack brackets in front handles on side trim recesses using M4 x 16 panhead screws and washers, finally refit top and bottom covers.

Chapter 3-1

OPERATION

PREPARATION FOR USE

Providing the instrument is properly adjusted for AC supply voltage and is connected to an outlet socket with the correct fuses fitted, the instrument can be switched on.

At switch-on, a self test operation which checks the instrument's memory is applied. Should the instrument fail the self test, LOCAL and SHIFT LEDS will flash alternately and a message descriptive of the fault together with the CRT test pattern will remain on the screen (see Fig. 3-1). The last digit "n" in the code M6500/A15/IOn is the instrument's firmware issue number. If it is necessary to establish this number, a fault should be simulated by holding down any key other than MARKER as power is applied. The firmware issue can then be noted.

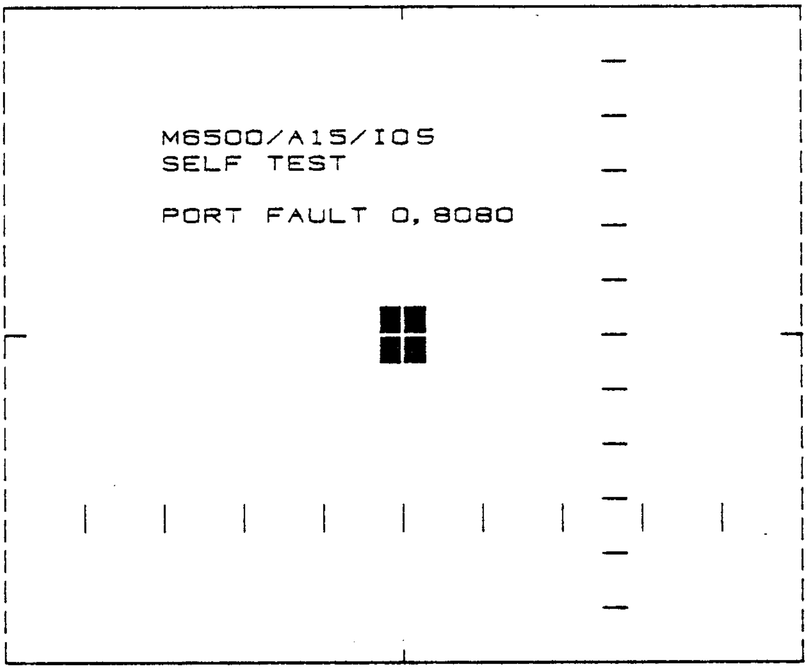


Fig. 3-1 Test pattern display and self test fault indication.

If the instrument is functioning correctly the LOCAL LED will remain on, the SHIFT LED OFF and a display of power on channel A will be shown. The fault messages are more fully explained in Chapter 5 of the Service Manual under "Processor faults (AC18) - Self test fault displays"

Note ...

If the power-on mode does not initiate the correct display or if the GPIB/LOCAL LED remains off; switch the power off, wait 10 seconds and repeat the switch on procedure.

To remove any small DC voltages, a zero operation must be performed before any measurements are made and this must be carried out with all required probes connected and the RF switched off. (See Miscellaneous secondary functions - ZERO key, Chap. 3-1 for details).

Although particularly suited for use with 6300 series sweepers, the 6500 can control any microwave sweeper capable of accepting an external ramp control. Two voltage ramps are available, a fixed 0 to 10 V and an adjustable 0 to 20 V, either may be connected via the rear panel BNC terminations. In some cases special terminations, connectors or cables are necessary to couple the 6500 to the sweeper; these can be supplied as optional accessories complete with fitting instructions.

Once this connection has been made the 6500 should be initialized to the sweeper by entering the F1 and F2 settings on the 6500 (the F1 and F2 frequencies are those obtained from the sweeper when the external ramp is at its minimum and maximum respectively). To facilitate this procedure, the ramp is moved to the bottom and top of its range when the prompts for setting F1 and F2 appear on the 6500 screen. This allows the use of a frequency counter so that measured frequencies can be entered. This is especially useful when frequencies generated under external ramp control can be affected by the front panel controls of the sweeper.

In addition to the frequency control one further connection may be necessary, If a multiband sweeper is being used then it is desirable to pause the sweep when the bandswitch points occur to avoid errors due to the delay between one oscillator stopping and the next starting. This can be accomplished by connecting the SYNC input on the rear panel of the 6500 to the appropriate blanking output of the sweeper. A single BNC lead is required. Fig. 3-2 shows the connections to a typical sweeper and a counter. The titles of input and outputs on particular sweepers are listed on the next page.

Note ...

For details of operation with 6300 series sweepers, consult the appropriate sweeper operating manual.

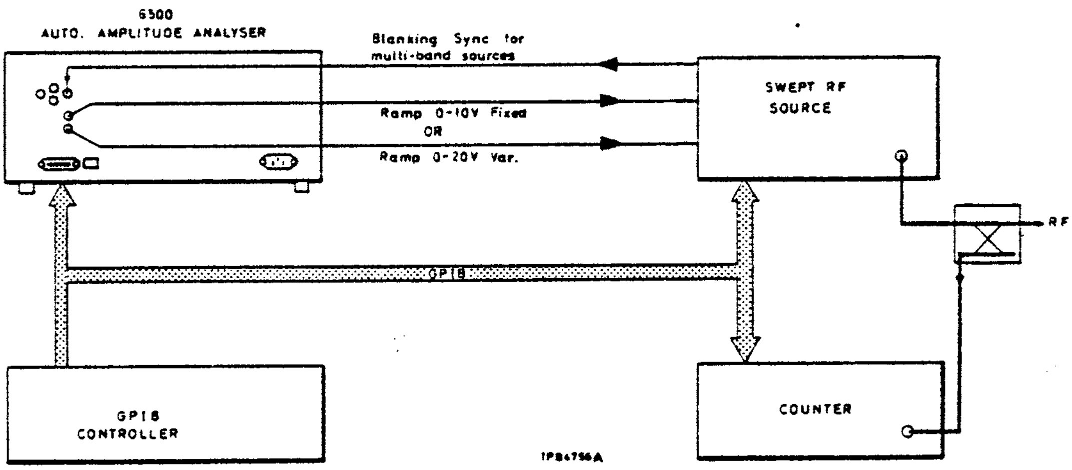


Fig. 3-2 Connections to Swept RF Source and Frequency Counter

RF Source		Comments		
Manufac.	Type	Ramp Input	Rear Panel	Front Panel
Marconi Instruments	6300 Series	0-10 V	Use Sweep input	See appropriate manual for set-up details.
"	6600A/1	0-20 V approx.	(See additional info. overleaf)	Use Ext Sweep input. Set Sweep/CW to EXT.
"	6158A & 6150 Series	0-10 V	Use Sweep Input	Set Function to SWP. (Not CW or AM)
Hewlett Packard	8690 Series	0-20 V	-	Use EXT FM Input Note: Need 0 to +17.5 V for fullband sweep.
"	8620C Series	0-10 V	Use Pin 28 and 43 (ground) on Socket J2 or MI Interface cable Part No. 3964-003. Use Sync on multiband plug-ins.	Set Sweep Mode to EXT. Note: Under GPIB or ramp control it may be better to use Start/Stop etc. Marker sweep with markers set by counter. Note also no local lockout of HP8620C Front Panel Controls.
"	8350A Series	0-10 V	Use Blanking Sync on Multi-band plug-ins.	Set Sweep to EXT. Connect ramp to Sweep input. Note: Sweep input and output are same BNC socket Note: Under GPIB Control set F1 and F2 on 6500 and then put into FREEZE mode. Using Brightline at start adjust 8350A start frequency for desired reading on counter. Repeat for Stop Frequency. This method locks out 8350A. Controls and offset and gain errors of 6500 ramp are calibrated out.
Wiltron	610D Series	0-20 V Set 0 to 9.75 V	Open link BC. Use terminals B & D. Use Blanking Output during Bandswitch for Sync. (B is signal, D is ground).	Set Freq. Program to External. Note: If fitted with GPIB (option 16) use SYNTH mode described in Operating Manual Vol. 1a, or details of a simple modification can be provided on request.
"	6600 & 6600A Series	0-10 V	Use BNC EXT Sweep Input. GPIB (Opt.3)	Set Ext Sweep Note: See Under 8350A for GPIB marker sweep.

Using Automatic Amplitude Analyzer type 6500 to control Microwave Sweep Oscillator MI 6600A/1

The 6600A/1 sweeper is designed to respond to an external sweep unit in the range 0-20 volts but the RF frequency of the plug-in unit is clamped at both ends. Consequently, the nominal frequency range starts at a point corresponding to an input voltage slightly above 0 V and ends when that input voltage reaches a point somewhat below 20 V.

To facilitate initial setting up of the F1 and F2 limits on the 6500, the following table has been prepared. It represents the low and high frequencies which would correspond to input voltages 0 and 20 respectively, if the oscillator were capable of reaching them. They are termed the 'VIRTUAL LIMITS'.

If the full 0-20 V output ramp from the 6500 is applied to the EXT SWEEP input of the 6600A/1 and the Virtual limits are set into the 6500 as F1 and F2, horizontal frequency scaling and BRIGHT LINE read-out will be correct for all valid frequencies (i.e. within the nominal band of the plug-in unit).

6600 SERIES PLUG-IN UNITS

RF Source Type Numbers	FREQ. RANGE (GHz)	VIRTUAL LIMITS (GHz) Low	High
6608-6611	1.0 - 2.0	0.925	2.13
6612-6615	1.4 - 2.5	1.375	2.58
6618,6619	1.7 - 4.2	1.49	4.49
6620-6623	2.0 - 4.0	1.85	4.25
6673,6674	2.0 - 4.5	1.80	4.80
6624-6627	3.5 - 6.75	3.39	6.98
6630,6631	3.7 - 8.3	3.60	8.40
6632-6635	4.0 - 8.0	3.70	8.50
6658	4.8 - 9.7	4.44	10.20
6636-6639	7.0 - 11.0	6.70	11.50
6640-6643	7.0 - 12.4	6.75	12.75
6676	7.0 - 13.0	6.59	13.14
6677	7.0 - 16.0	6.70	16.30
6644-6647	8.0- 12.4	7.85	12.65
6666	8.0 - 16.0	7.40	17.00
6667	8.0 - 18.0	7.25	19.25
6648,6657	10.0 - 15.5	9.80	15.80
6668	10.0 - 20.0	9.25	21.25
6649,6653	12.4 - 18.0	12.20	18.20
6670	15.0 - 22.0	14.9L	22.11
6650	18.0 - 26.5	17.60	27.20
6651	26.5 - 40.0	26.31	40.60
6659	33 - 50	32.20	51.40
6654	40 - 60	38.50	62.50
6671	50 - 75	48.00	78.00
6655	60 - 90	57.75	93.75
6672	75 - 110	74.63	110.63
6669	75 - 120	73.50	121.50

FRONT PANEL CONTROLS

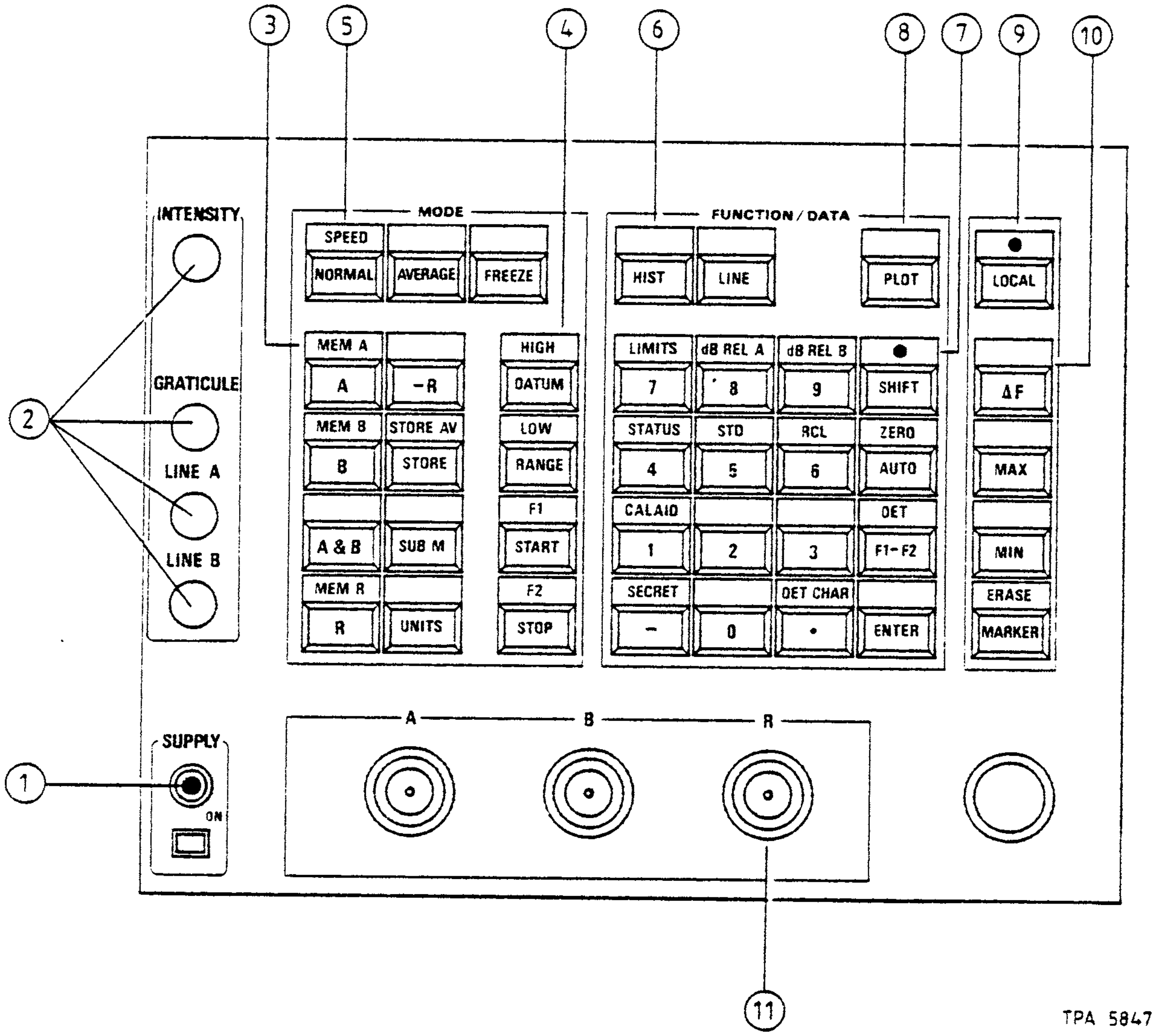


Fig. 3-3 Front panel controls

(1) SUPPLY

Push button switch applies the AC supply voltage to the instrument for both manual and remote control operation. An associated lamp indicates that power is on.

(2) INTENSITY controls

INTENSITY adjusts the overall brightness of the display. **GRATICULE**, **LINE A** and **LINE B** control the relative brightness of these three traces.

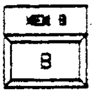
MODE KEYPAD

(3) Measurement mode keys

These keys select combinations of the measurement channels (A and B) and the reference channel (R) for display and storage. Units of power measurement may also be defined. The functions of the individual keys are outlined below.

[A] Displays channel A.

[MEM A] Displays contents of memory A.



[B] Displays channel B.

[MEM B] Displays contents of memory B.

Displays channels A and B.

[R] Displays channel R.

[MEM R] Displays contents of memory R.

Subtracts channel R from selected measurement before display.

[STORE] Used with [A], [B], [A&B] and [R] keys to store current display to memory A, B or R. [STORE][A&B] can only be used when channels A and B are displayed, the traces being stored to memories A and B respectively.

[STORE AV] Used with [A], [B], [A&B] and [R] keys to store the **average** of the current display and the current contents of the selected memory to this memory. [STORE AV][A&B] can only be used when channels A and B are displayed; the two channels being averaged with and then stored to memories A and B respectively.

Used with keys [A], [B] and [R]. [SUB M][A] subtracts the contents of memory A from channel A whenever this is displayed. Similarly for [SUB M][B]. [SUB M][R] subtracts contents of memory R from channels A and/or B. No memory can be subtracted from channel R.

Switches between dBm (default) and mW scaling for absolute power measurements; dB (default) and VSWR for relative measurements.

(4) Scale keys

These keys define the scaling and limits of the power and frequency displays.

[DATUM] Used with numeric keys to define power level at top of display (within range ± 99.9 dBm).

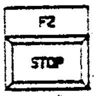
[HIGH] Used with numeric keys to define high power limit (within range ± 99.9 dBm). Exceeding limit causes a warning message to be displayed.

[RANGE] Used to define power scaling (range: 0.1 to 10.9 dB(m) per division).

[LOW] Used to define low power limit (within range ± 99.9 dBm). Exceeding limit causes a warning message to be displayed.

[START] Used to define start frequency for sweep.

[F1] Used to define (enter) minimum frequency available from sweeper.

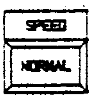


[STOP] Used to define stop frequency for sweep.

[F2] Used to define (enter) maximum frequency available from sweeper.

(5) Sweep control keys

These keys are used to select sweep speed, normal or averaged display, and the "freezing" of the display.



[NORMAL] Selects normal sweeping. Measurements are made at each of 422 positions across the screen and directly displayed. Normal sweeping is the default (power-up) mode.

[SPEED] Used to define the sweep speed. Ten speeds are available, ranging from 70 ms up to 20 s.

Selects display averaging and (re)starts averaging process.

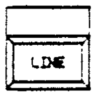
Freezes display to allow it to be photographed.

FUNCTION/DATA KEYPAD

(6) Display keys

Used to select line or histogram display for channels A and B.

Preceded by A or B, selects histogram display for corresponding channel.

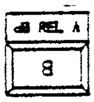


Preceded by A or B, selects line display for corresponding channel.

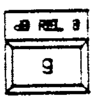
(7) Miscellaneous functions and numeric keypad

The numeric keypad (digits 0-9, minus sign and decimal point) consists of the primary (unshifted) functions of 12 of the 16 keys in this group. As their numeric function is self-explanatory, these keys are only referred to where they have a second (shifted) function associated with them.

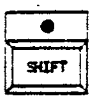
[LIMITS] Used to enable/disable (toggle action) limits previously set using the [HIGH] and [LOW] keys.



[dB REL A] Allows a 0 dB offset to be set for the channel A trace. This may be at either the current bright-line power level, or (by entering the appropriate numeric value) at any other level in the range ± 99.9 dBm.

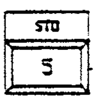


[dB REL B] As [dB REL A] but for channel B.

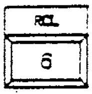


Selects shifted functions. Remains active until another key is pressed. Active state is indicated by illumination of integral LED.

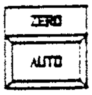
[STATUS] Various status information is presented on the CRT. This includes limit values (and whether or not limits are enabled), dB offsets (as entered via dB REL A or dB REL B), GPIB address, detector status (i.e. which detectors are connected).



[STO] When followed by memory number 1 to 9, stores current instrument settings to the appropriate memory.



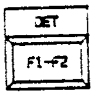
[RCL] When followed by memory number 1 to 9, recalls previously stored instrument settings from the appropriate memory.



[AUTO] Automatically selects values of RANGE and DATUM to give optimum display on the screen.

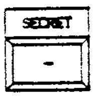
[ZERO] Automatically zeros any sensor connected.

[CALAID] Used in calibration to set up the signal channel. The display obtained (of power level and range) is also useful as a confidence check.



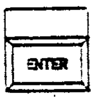
[F1-F2] Selects full sweep: F1 to F2.

[DET] Allows detector type to be specified. 6511/12 type is default.



[SECRET] Removes frequency scale from display for security. Toggle action.

[DET CHAR] Allows entry of characteristics of non-Marconi Instruments detectors.



Causes entry of numeric values.

(8) PLOT key

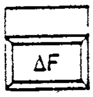
Activates X-Y plotter controls to produce hard copy of displayed results.

(9) LOCAL key

Returns instrument to local (manual) control from remote (GPIB) control. Integral LED illuminated indicates local control.

(10) BRIGHTLINE controls

The "brightline" is a vertical line extending from top to bottom of the screen, which defines the point in the sweep for which the power level and frequency are digitally displayed. At switch-on the brightline is coincident with the power axis on the left-hand side of the screen. The brightline controls (1) allow the brightline to be positioned manually or automatically at significant positions on the displayed trace, (2) define the brightline position as the center point in a sweep (3) allow markers to be placed at significant positions.



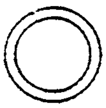
Allows the sweep width for a symmetrical sweep about the brightline position to be defined. Value entered is the total sweep width.

Sets brightline to maximum power position.

Sets brightline to minimum power position.

[MARKER] Places marker (a static brightline) at the brightline position. Up to eight markers may be set in this way. When the brightline is placed over an existing marker, this key causes that marker to be erased.

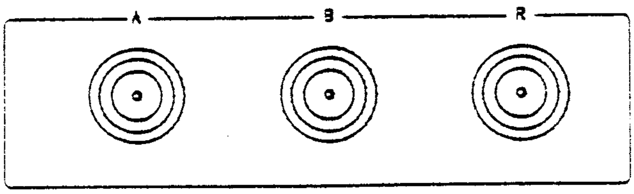
[ERASE] Erases all markers.



The rotary control is used to manually position the brightline. There is no mechanical limit on this control.

(11) Channel input connectors

Connectors A, B and R accept 12 pin plug connectors from the detector cable assemblies for channels A, B and R.



REAR PANEL CONTROLS

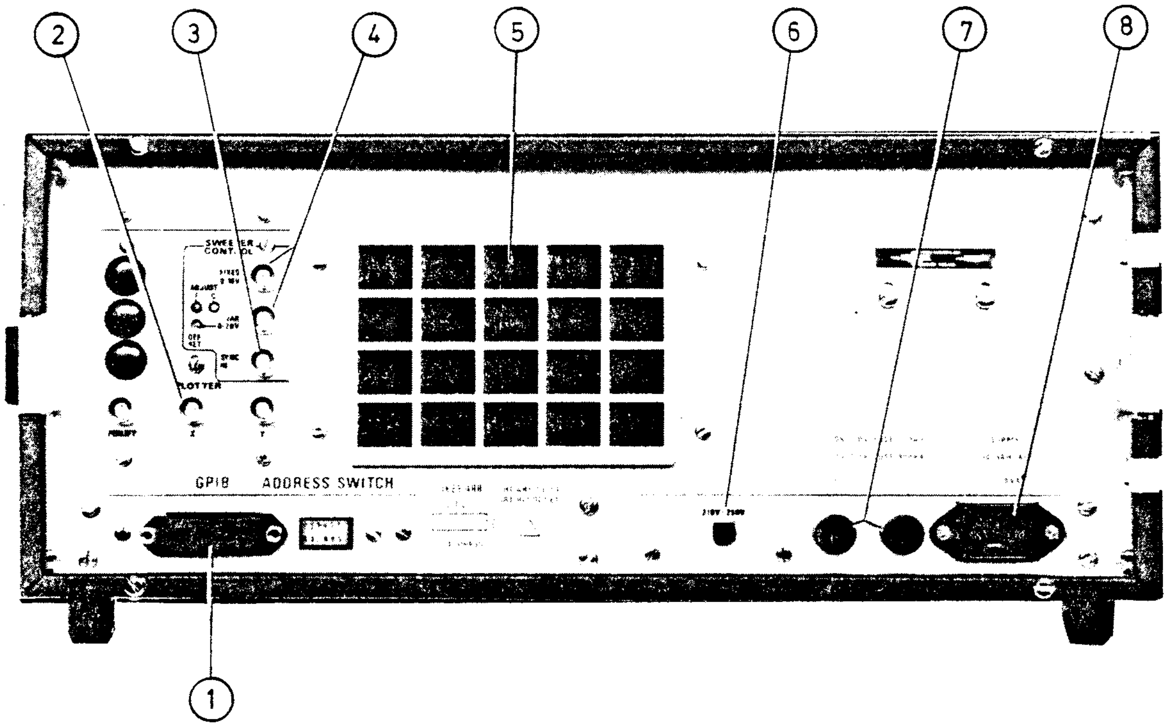


Fig. 3-4 Rear panel controls

(1) GPIB Interface

This option (available built-in or as an accessory) allows remote control ot the instrument and accepts the standard 24-way IEEE GPIB connector. An adaptor, Code No. 46883-408K is available for IEC 625 systems. The interface can also be used to facilitate stand alone digital plotting if required.

(2) PLOTTER

By connecting the X,Y and PEN LIFT outputs to a standard X.Y recorder a plot of the current traces plus graticule and scaling information can be provided. The PEN LIFT output is usually closed circuit for pen down and open circuit for pen up; this can, however, be reversed by the user if required by following screen prompts when PLOT key is pressed.

(3) SYNC IN

When this socket is connected to the appropriate socket of a multiband sweeper, correct operation at the bandswith points is ensured. A High level (3 to 5V) or Low level (- 3 to - 5V) from the sweeper will pause the 6500 sweep while this sync level is maintained. When the voltage at this input returns to 0V the sweep will continue. Using this input it is possible to stop the 6500 sweep for up to 600 ms at any one measurement point.

(4) RAMP

(i) FIXED 0- 10 V. This output provides the necessary control voltage to drive the sweeper. When sweeping from F1 to F2 as set on the 6500 this output will sweep from 0 to 10 V. When different start and stop frequencies have been selected this output will sweep across correspondingly different voltages.

(ii) VARIABLE 0 - 20 V. The variable output provides the same function as the fixed ouput, but is for connection to sweepers which require a different drive level. The maximum range of this ramp output voltage can be adjusted using the **C** (coarse) and **F** (fine) screwdriver adjustment controls. The starting point of this ramp output can be adjusted by the **OFFSET** screwdriver control between ±10% of its maximum setting. This operation may need more than one iteration.

(5) Fan air vent

Forced air cooling is used to maintain the required operating temperature within the instrument, therefore allow at least 75 mm (3 in) clearance at the rear of the instrument and ensure that the air vents are not obstructed. The cooling fan requires no maintenance although the air filter should be cleaned at regular service intervals.

(6) AC supply locking plate

The instrument is normally despatched with the plate locking the supply selector switch to the 210-250 V position. To change to 105 - 120 V operation, remove the locking plate, adjust the switch, reverse the locking plate and refit.

(7) AC supply Fuses

Supply input fuses are rated at 600 mA-T for 210-250 V operation or 1.25 A-T for 105-120 V operation.

Note ...

The instrument employs double fusing, and should the fuse in the neutral line rupture certain areas in the instrument may remain at mains potential.

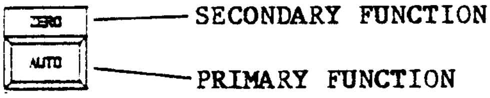
(8) AC supply input

Accepts AC supply input of 50-60 Hz; the earth pin is internally connected to chassis.

OPERATING PROCEDURE

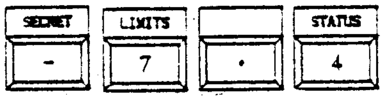
Introduction - key operation

All operations are carried out via the front panel keyswitches (or GPIB if fitted) which are used to enter commands and numerical values. Many keys have two functions, the secondary function being indicated on the top half of the push-button.



The secondary function is obtained by pressing the SHIFT key followed by the required second function key. Pressing any further key (including SHIFT) extinguishes the the SHIFT key's integral LED and cancels the secondary function mode.

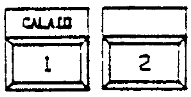
Any command which requires numeric data to follow it produces a prompt or selection menu on the display. When the prompt is displayed the numerical data should be typed in followed by ENTER. For example, to set a HIGH limit of -7.4 dBm:

Parameter selection	Prompt	Numeric entry	Terminator
	**Set High Limit**		

As ENTER is pressed, a terminator (dB(m) in this case) is displayed on the screen to confirm that the entry has been accepted. This will remain as long as the key is held down. If a mistake is made at any point the command can be entered again simply by starting the sequence again. If an ERROR message results, this indicates that an illegal input was attempted, e.g. attempting to set RANGE in excess of 10.9 dB(m) per division:-

Prompt

Set Range



This will produce the message **Error 12 ** meaning "Entry overflow". Other error codes used in 6500 are given in Table 3-1.

TABLE 3-1 ERROR CODES

GENERAL OPERATING ERRORS	
01	Attempt to enter more than eight markers.
02	Sweep data was invalid when last operation attempted.
03	Attempt to recall instrument settings from null memory.
04	Relative measurements on R channel (SUB M and -R not allowed).
05	ΔF sweep width greater than F1-F2 range.
KEYBOARD ENTRY ERRORS	
11	Negative entry not allowed for attempted operation.
12	Entry overflow.
MEMORY ENTRY ERRORS	
21	Memory start/stop frequencies different to current screen settings.
22	Attempt to subtract null memory.
23	Attempt to use STORE AV on null memory.
24	Attempted memory operation on incorrect channel. (See table of valid operations).
GPIB ERRORS	
	For details of GPIB errors see GPIB Operating Manual Vol. 1a.
HARDWARE ERRORS	
41	Keyboard fault.
42	ZERO fail. Caused by defective probes or RF present.
43	Timeout on D/A read. (No valid range).
44	Timeout on SYNC. input. (Check sweeper).
45	Maximum RF input level exceeded.
46	Detector temperature range exceeded.

Where an entry is made which can be independently set on the three channels, the entry will only affect the channels which are currently selected as indicated by the brightline power reading(s) at the top of the display:

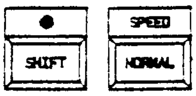
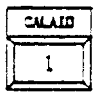
SELECTED
CHANNELS

e.g. A = - 12.34 dBm B = - 56.78 dBm

Both A and B channels (but not R) will be affected by the entry.

When a selection menu is displayed, or example in setting the sweep SPEED or PLOT modes, the appropriate numeric key should be pressed. No ENTER key is required.

e.g. Set sweep SPEED of 100 ms:-

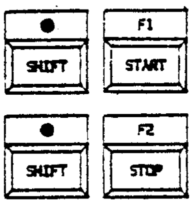
Parameter Selection	Sweep speed selection menu		Selection
	0 - 70 ms	5 - 1 s	
	1 - 100 ms	6 - 2 s	
	2 - 200 ms	7 - 5 s	
	3 - 300 ms	8 - 10 s	
	4 - 500 ms	9 - 20 s	

Select Option

When the instrument is first switched on, F1 and START will automatically be set ot 0.01 GHz, and F2 and STOP to 18 GHz. Before any measurements are made, the F1 and F2 parameters of the sweeper being used should be entered, otherwise an incorrect frequency display will result. A frequency counter may be used to facilitate more accurate settings see Fig. 3-2. The procedure is:

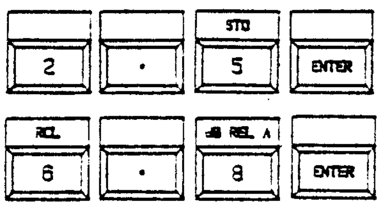
(a) Select [SHIFT] [F1] and read the frequency counter e.g. 2.5 GHz
(b) Enter this value and terminate using the ENTER key.
(c) Select [SHIFT] [F2] and again check the counter e.g. 6.8 GHz
(d) Enter this value and again terminate using the ENTER key.

Prompt



Set Sweeper F1

Set Sweeper F2



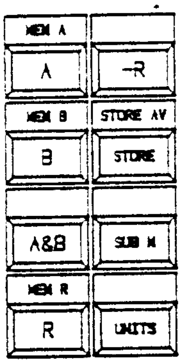
Note...

If at any time the relationship F1, < F2 < 126 GHz is not maintained, the entry will be rejected and ** Error 12** message is displayed. When this happens set F2 first, then F1.

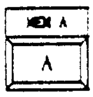
This sequence will also set START and STOP to F1 and F2 so a full width sweep of F1 to F2 will result.

KEYSWITCH FUNCTIONS

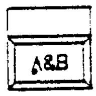
Measurement mode keys



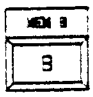
The purpose of these keys is to select the required channels and memories appropriate to the measurement being made. The mode should be set up by first selecting one of the four options:-



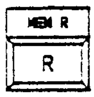
Select Channel A for display



Select Channels A & B for display



Select Channel B for display



Select Channel R for display

The above keys are independent and will initially provide a swept display of power on the selected channel(s). At switch on, the display is set automatically to channel A in dBm. The UNITS key allows the user to select a display in either dBm or mW (toggle action). Note that the mW scale is fixed at 0 - 5mW and cannot be altered in either RANGE or DATUM.

Switches between dBm (default) and mW scaling, if measurement is of absolute power.

To indicate that an ´absolute power´ mode (Channel A, Channel B or Channel A&B) is selected, the plot title "Power" will appear at the top of the screen, and the units will be displayed at the top of the Power axis. The power at the brightline position is shown below the plot title for each selected channel, e.g.:

A = +16.7 B = -49.32 dBm (See Chap. 1, Page 2, Fig. 1-1)

Since no sweeper´s output is perfectly flat across its frequency sweep it is often necessary to cancel the variation in output level of the sweeper to obtain a true display of the response of the device under test. This is achieved in the 6500 by the provision of a live Reference channel. The reference channel detector and measurement channel(s) detector(s) are connected to the same sweeper, and the reference channel´s response is simply subtracted from that of the measurement channel(s) by selecting the [-R] key.

In this way, any variation in the sweeper's output is removed from the measurement.

Subtracts response on channel R from selected measurement channels before display to screen.

When [-R] is selected (e.g. with A&B) it will be indicated by the title:

Gain/Loss Channel A&B (-Ref)

whenever the live Reference mode is selected it will be indicated in the title by "(-Ref)".

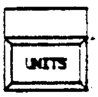
Note...

(1) Loading effects may cause variations in the output of an inherently "flat" sweeper which would also necessitate the subtraction of the reference channel to give a true response for the device under test (DUT).

(2) No relative (dB REL) or gain/loss (-R) measurement may be made on Channel R itself. Any attempt to do so results in an * * Error 04 * * message.

(3) Before any measurements are displayed in this mode, a sweep must be made on the R channel. This is not displayed but will be noticed as a delay before a trace appears.

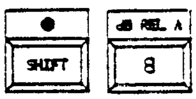
The scaling represents the difference in absolute power levels between channel R and channels A,B or A&B and will be displayed in dB. If the measurement system is such that this represents a VSWR, the scaling can be changed via the UNITS key to give a VSWR range of 1.0:1 to 3.0:1. This is a fixed range and cannot be altered by RANGE or DATUM.



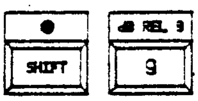
Switches between dB (default) and VSWR scaling if measurement is gain/loss or relative (A/B or A&B -R)

An additional facility is provided by the dB REL A and dB REL B keys. The two keys, (one for each measurement channel) allow the user to select a 0 dB reference either at the current brightline reading, or at any other level by selecting a numeric offset. Both keys act independently to allow different positions to be set on the two measurement channels.

Prompt



or



Enter offset dB Rel A (or B)

If the ENTER key is pressed with no number entry the current brightline reading is made a 0 dB reference. Alternatively the required numeric offset may be entered followed by the ENTER key to terminate the entry. The STATUS display will show the current values of offsets entered for both A and B channels. (See paragraph on STATUS key).

When an offset has been entered, the title will become

dB Relative

If in addition, the live Reference mode has been selected, this will again be indicated :

dB Relative (- Ref)

Note ...

> It is possible to perform a dB Relative function on only one trace when two channels are simultaneously displayed. This allows absolute power (dBm) and Relative measurements (dB) to be displayed at the same time; the title will, however, remain as above.

Memory operation

The STORE key and the SUB M key in the mode block refer to the three available memories (A, B or R), which are each capable of storing a complete sweep of 422 measurement points.

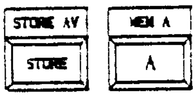
Each of the operating modes previously described may be modified by use of these memories. For instance, the frequency response of a device may be removed from future measurements by first storing the response ([STORE] A,B, or R) and then subtracting the stored values from the live display ([SUB M] A,B or R). This procedure is known as "normalisation".

In all cases, whenever a memory is being subtracted from a measurement, it is indicated on the title by the memory name (A, B or R) in brackets, e.g.

Gain/Loss (- A,R)
indicates 'A' and 'R' memories are subtracted.

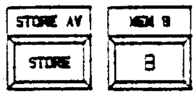
dB Relative (-Ref) (-B)
indicates dB relative mode with live reference and the contents of memory 'B' being subtracted before display.

The STORE key allows the current trace(s) to be stored to memory. When pressed, the prompt **Store to Memory** appears and the current sweep in progress will stop. This should be followed by a key as indicated below.



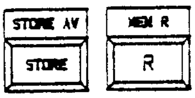
Stores current trace to Memory A.

This cannot be used when A & B are simultaneously displayed.



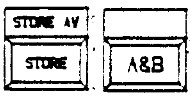
Stores current trace to Memory B.

This cannot be used when A & B are simultaneously displayed.



Stores current trace to Memory R.

This cannot be used when A & B are simultaneously displayed.



Stores current Channel A trace to Memory A, and Channel B trace to Memory B. Only use when A and B are simultaneously displayed.

Pressing 'NORMAL' cancels STORE mode, and sweep continues without any change to operating mode or memory.

An additional facility is provided to average the contents of a memory with a current trace, and store the result. This is achieved by preceding the above keystroke sequences by SHIFT. This accesses the store average facility, and the prompt

AVERAGE TRACE TO MEMORY

will appear. The operation remains the same as STORE but with the difference that the current trace is averaged with selected memory before it is stored to it.

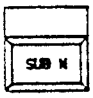
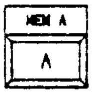
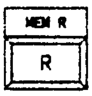
e.g. 

average current trace with memory A and store result to memory A.

Note ...

** Error 23 ** message is produced if an attempt is made to STORE AV to a memory which has no contents. The function is, however, performed assuming contents to be zero. No STORE is allowed in VSWR or mW units.

The operation of the SUB M key is as follows:-

Parameter Selection	Prompt	Terminator	
	**Subtract Memory**		Subtract memory A from trace A. Use whenever Channel A is displayed.
			Subtract memory B from trace B. Use whenever Channel B is displayed.
			Subtract memory R from trace A and/or B as selected. Use whenever Channel A and/or B is selected.

Note ...

(1) No memory can be subtracted from Channel R.

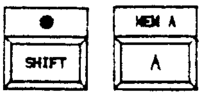
(2) Memory R is subtracted from both Channels A and B if these are displayed when [SUB M] [R] is selected.

(3) It is not possible to subtract Memory A from trace B or vice-versa.

(4) Message ** Error 22 ** will be generated if an attempt is made to subtract a memory with no contents.

Valid memory operations are summarized in Table 3-2. Any attempt to select the memories in a way other than those listed will result in an ** Error 24 ** message being displayed. The contents of any memory may be examined at any time by pressing SHIFT followed by the channel memory required.

e.g.



Displays Memory A.

TABLE 3-2 VALID MEMORY OPERATIONS

CHANNEL	A	B	A & B	R
Store trace to memory	A B R	A B R	A to MEM A B to MEM B	A B
Subtract Memory	A R	B R	A B R	

Sweep control keys

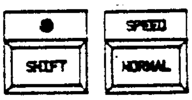
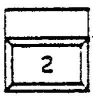
Two methods of sweeping are available: NORMAL and AVERAGE. When [NORMAL] is selected, measurements are made at each of the 422 positions across the screen, displayed and directly stored to the appropriate display memory. (N.B., **not** the selectable channel memories accessed via STORE). The AVERAGE key enable signal processing to provide noise reduction by averaging the current measurement with the contents of the display memory corresponding to the same ramp position. This is done for every measurement point and has the effect of reducing noise over consecutive sweeps. This process restarts whenever the AVERAGE key is pressed.

Selects averaging mode and restarts averaging process

Note ...

The averaging mode should be started when a steady trace is present. If changes in power level occur during a sweep in this mode, the trace will not return to a true representation of the measurement until many sweeps have occurred as it treats the changes as noise to be removed. If a change to the system is made, AVERAGE should be pressed again to restart the process. To cancel AVERAGE press NORMAL.

The actual number of measurements taken at each measurement point and consequently the sweep SPEED is selected by the secondary function as shown in the example below. A sweep speed of 200 ms is selected.

Parameter Selection	Selection menu	Selection
	**Sweep Speed** **0 - 70 ms** **5 - 1 s** **1 - 100 ms** **6 - 2 s** **2 - 200 ms** **7 - 5 s** **3 - 300 ms** **7 - 10 s** **4 - 500 ms** **9 - 20 s** **Select Option**	

Note ...

(1) No ENTER key operation is required to terminate the sweep speed entry.

(2) The speeds shown are nominal and will vary depending on power level,

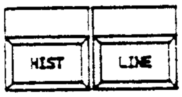
shape of trace and any delays introduced by sweep hesitation etc.

(3) The sweep speed and sweep mode selected are displayed on the screen in the top right corner.

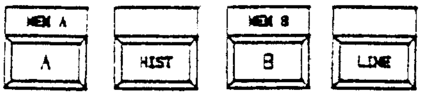
(4) Sweep speed 0 provides reduced resolution - only half the number of measurement points are taken with one measurement occupying two display points - but this gives a "real time" feel for adjustment or peaking of devices under test.

The FREEZE mode allows the sweep to be stopped for examination or photography. In this mode the ramp outputs on the rear panel will track any movement of the brightline allowing frequency accuracy checks to be made. This key has a toggle action, and pressing it again will cause the sweep to restart.

Display keys



There are two methods of presenting the trace on the screen, HISTogram or LINE format. This is for visual effect only and does not affect any operation of the instrument. It is useful when displaying two traces simultaneously to have them in different forms for easy identification of channels. When pressing the HIST or LINE keys, the selected channels are affected.

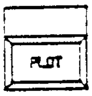


Sets up display of channel A in Histogram and B in line format.

Note ...

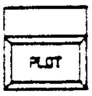
Channel R is displayed on the same format as selected for Channel A.

PLOT key



The 6500 has a facility enabling a hard copy of the display to be obtained using a standard X-Y (analogue) plotter. Three outputs are provided from the rear panel for connection to the X, Y and Pen-Lift inputs of the plotter. The X and Y outputs provide signals in the range 0 - 10 volts, while the Pen-Lift output is an open-collector drive.

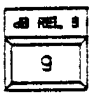
At any time when there is a complete trace available on the screen, press PLOT.



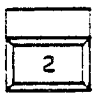
A selection guide is displayed covering all the facilities available in the PLOT mode. Selecting 0 will cause all three operations 4,5 and 6 to be carried out in sequence.

0 - Plot all
1 - Pen Bottom Left
2 - Pen Top Right
3 - Pen to Origin
4 - Draw Axes
5 - Label Axes
6 - Plot
7 - Set Pen Lift
8 - Set Plot Speed
9 - Set Live Y

Prompt



Set Live Y
1 - Off
2 - On



New display

Set Live Y ON

When Live Y is enabled the Plotter Y output voltage follows the screen update point during sweep operations. The top of the screen corresponding to 10 V and the bottom to 0 V. Resolution is 256 steps. The plotter Pen-Lift output is also set to pen down during ramp retrace. This facility may be used for RF blanking during retrace if desired.

1) The X and Y outputs are set to minimum, allowing adjustment of the plotter sensitivity and zero controls to give a position at the bottom left of the paper.

2) The X an Y outputs are set to maximum, allowing adjustment of the plotter sensitivity and zero controls to give a position at the top right of the paper.

3) When a plot is made space is allowed for labelling of the axes. If this is not required, this option allows the origin of the displayed trace to be set as opposed to bottom left ((1) above).

4) The X and Y axes are plotted including 'tick' marks indicating positions of the frequency graticule lines. Ticks are also provided to show the positions of any markers present, including the brightline.

5) The DATUM(s) and RANGE(s) are written to the left of the Y-axis, the DATUM(s) at the top. If two traces are being plotted, a pause is introduced when the data pertaining to the A trace has been written, allowing a pen change. When ready, press '1' as prompted to continue the labelling.

6) The displayed traces are copied to the plotter. If both A and B channels are selected, B is plotted first. After a pen change, if necessary, press the numeral 1 key as prompted to continue the plotting.

7) Set sense of pen lift drive. Normally pen lift output is high impedance for PEN UP. Select INVERT for low impedance for PEN UP. Options are presented as a separate prompt:

	Prompt		New display
LIMITS 7	Set Pen Lift 1 - NORMAL 2 - INVERT	CALAID 1	Set Normal (Pen lift operation)

8) When plotting and drawing alphanumerics the 6500 maintains the pen speed constant. Select pen speed from 1 to 9 (1 is fastest) to suit plotter slew rate. Prompt is displayed -

	Prompt		New display
dB REL A 8	Set Plot Speed (1 - 9)	CALAID 1	Set fastest speed

As each function is completed, the instrument returns to the initial selection guide to allow further instructions. To return to normal operation press NORMAL.

Note ...

'Digital Plot' facilities are available when using the GPIB Interface (Option 001). Details of this are given in the GPIB Operating Manual, Vol. 1a.

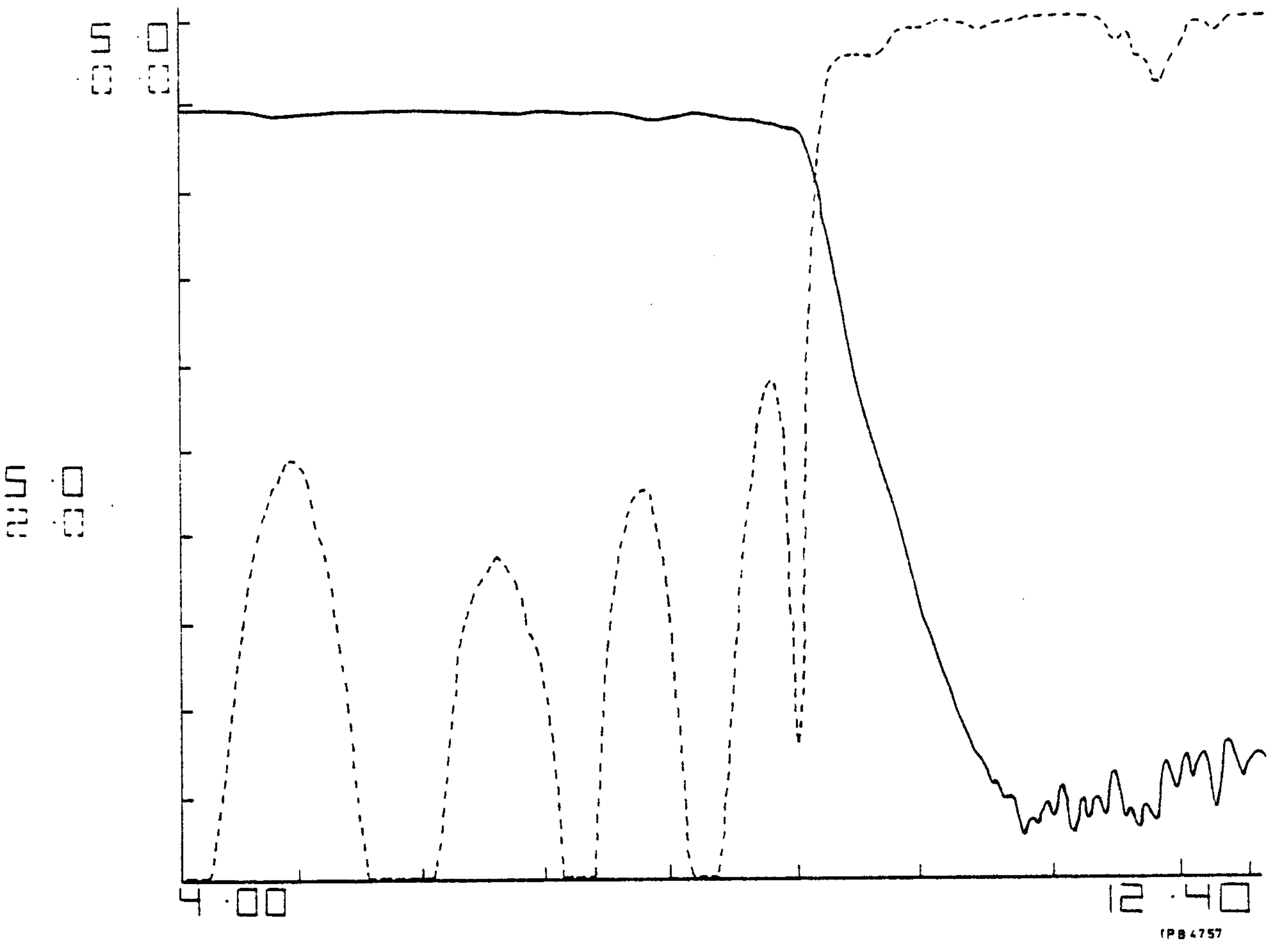
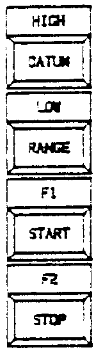


Fig. 3-5   Typical X-Y plotter presentation

Scale keys

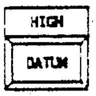


The four scale keys and their associated secondary functions allow operating parameters to be entered on the numerical keyboard. Two keys are used to set the power range and limits and two are used to set the frequency range.

Power range and limits

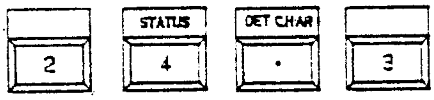
When the instrument is first switched on, the display shows an amplitude scale of + 20 to - 80 dBm (DATUM + 20 dBm, RANGE 10 dBm/division) on channel A. The instrument's total dynamic range of 100 dB is thus displayed. DATUM and RANGE can be entered individually for each channel A, B and R, and only the channels currently selected will be altered when the parameter is entered.

Set DATUM within range + 99.9 to - 99.9 dB(m), e.g.



Prompt

Set Datum

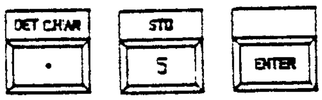


As each numeric key is pressed, the number is displayed to the screen until ENTER is pressed. whereupon their terminator 'dB(m)' will be displayed, showing the entry has been accepted. The entry may be abbreviated if no decimal data is required.

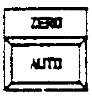
Set RANGE within range 0.1 to 10.9 dB(m)/division e.g.

Prompt

Set Range <dB/Div>



As each parameter is entered, the power scale will be adjusted and the sweep automatically restarted.



Pressing the AUTO key will automatically select values of RANGE and DATUM to give optimum display of the screen contents.

Note...

Pressing RANGE or DATUM keys will have no effect when displaying VSWR or mW scaling.

Different HIGH and LOW limits may be entered for the A and B channels.

If the LIMITS facility has been enabled (as indicated by an 'L' on the top left corner of the screen) each complete sweep will be checked to ensure it is within the present limits for that particular channel. If any point in the trace exceeds these limits, a message is displayed at the top of the screen indicating which limits have been exceeded. If, on a following sweep the power level returns within the limits, the message is erased and replaced with the original title.

To set level limits, first select the channel that the limits will apply to, and then enter as for DATUM or RANGE (above) but precede the sequence by SHIFT.

e.g. Set HIGH limit of ±99.99 dB(m):

SHIFT (●) | DATUM (HIGH) | Prompt: **Set High Limit** | 2 | 0 | • (DET CHAR) | 6 (RCL) | ENTER

These limits will be stored until new values are entered, even if the LIMITS facility is disabled.

Frequency range

The frequency information presented on the bottom line of the display is calculated assuming a linear response from the sweeper to the 6500's external ramp. To obtain a frequency reading at all brightline positions, the frequencies generated by the sweeper at the top and bottom of the range of the applied ramp must be entered into the 6500. These frequencies are termed 'F1' and 'F2' respectively. Providing the sweeper is stable, it should only be necessary to enter these values once.

e.g. Set up X-band sweeper.

SHIFT (●) | START (F1) | Prompt: **Set Sweeper F1** | 7 (LIMITS) | • (DET CHAR) | 9 (dB REL B) | 6 (RCL) | ENTER

When the prompt **Set Sweeper F1** is displayed, the ramp is set to the bottom of the range. Confirmation of the low limit F1 frequency is best obtained by reference to a frequency counter connected as shown in Fig. 3-2.

SHIFT (●) | STOP (F2) | Prompt: **Set Sweeper F2** | 1 (CALAID) | 2 | • (DET CHAR) | 3 | ENTER

Here the ramp is set to the top of the frequency range and this frequency is again best confirmed by using a frequency counter.

Note ...

(1) Some sweepers have front panel controls which affect F1 and F2 even when driven by an external ramp. If these are adjusted after the 6500 has been set up the frequency information may be incorrect.

(2) When using the variable 0-20V ramp, a DVM may be necessary to check

for correct ramp output voltage limits when adjusting the 'coarse' and 'fine' screwdriver controls.

(3) If an attempt is made to set F2 <F1, ** Error 12 ** message is displayed.

Once the 'F1' and 'F2' parameters have been set, it is possible so select any portion of this range to correspond to a full sweep on the 6500. As there are 422 measurement points and 4096 possible ramp points it is possible to expand the frequency scale approximately ten times without any significant loss in resolution. To select the required frequency band, use 'START' and 'STOP'.

Set a band of 9 - 10 GHZ (F1 and F2 previously set at 7.96 and 12.3 GHz).

[F1 / START] Prompt Set Start Frequency [dB REL B / 9] [ENTER]

[F2 / STOP] Prompt Set Stop Frequency [CALAID / 1] [0] [ENTER]

As each parameter is entered, the alphanumeric scaling and frequency related graticule lines are adjusted .

Note ...

(1) An entry will be rejected as an error if the condition

F2> STOP> START> F1 is not met.

(2) Frequency graticule lines will not be generated for sweep widths less than 100 MHz.

The BRIGHTLINE may also be used for setting START and STOP making numeric entry unnecessary.

e.g. Press START key and move the BRIGHTLINE to the required start point.

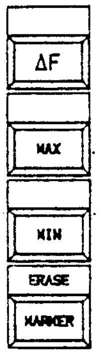
[F1 / START] Prompt Set Start Frequency [ENTER]

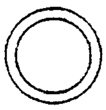
Note ....

As enter is pressed, the brightline frequency is copied to the screen and the terminator 'GHz' displayed showing the entry has been accepted. The BRIGHTLINE is also moved to maintain its frequency position: to the far left for START and to the far right for STOP.

In addition the ΔF key may be used to set symmetrical sweeps, this is discussed under the BRIGHTLINE Keys section.

Brightline controls

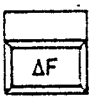




The "brightline" appears on the display as a single vertical line with a highlight "pip" at its base to distinguish it from any frequency markers. It can be moved horizontally to any position within the graticule using the rotary control at the bottom right of the instrument. The brightline is used to provide single spot measurements displaying both the frequency and amplitude of the measurement(s), where it intersects the trace(s). The spot measurements are derived from the internal data store, and are therefore unaffected by front panel range settings. Full resolution is always presented. Movement of the brightline is prevented during the first sweep after the measurement has been restarted, so as to ensure that the brightline will not display invalid data from previous sweeps. This inhibition of brightline movement is only noticeable on very slow sweep speeds.

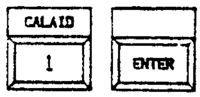
The position of the brightline can be used for setting START and STOP frequencies (as described under "Scale keys") and also for entering symmetrical sweep widths using the ΔF key, e.g.:

Set total sweep of 1 GHz about brightline position.



Prompt

Enter Sweep Width



At the prompt **Enter Sweep Width**, move the brightline to the point about which a symmetrical sweep is to be made. Select [1]. On pressing the ENTER key a 1 GHz sweep about the position of the brightline is obtained.

The scaling of the frequency graticule lines and the START and STOP parameters displayed on the screen will be adjusted, and a new sweep will be started.

Note ...

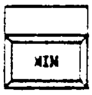
> If a sweep width is entered which would generate an illegal START and/or STOP frequency, the 6500 will only sweep up to the limiting frequency and the sweep will therefore not necessarily be symmetrical about the brightline position.

MIN/MAX Keys

The MAX or MIN keys are used to identify maximum and minimum level points in the currently displayed sweep(s). When one of these keys is pressed, the sweep update is stopped and the brightline moved to the maximum or minimum position appropriately. The **measured** max/min point is always selected regardless of whether this point is actually displayed, or of the relative positions of two traces on the display. The brightline spot measurement data is also updated.

e.g. To find maximum and minimum point:

Brightline is automatically moved to maximum data point on current trace and amplitude and frequency information is updated.

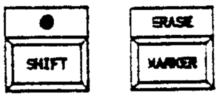


Brightline is automatically moved to minimum data point on current trace and amplitude and frequency information is updated.

MARKER key

Markers identical in form to the brightline (except that they do not extend below the bottom of the graticule) may be positioned anywhere within the graticule to identify important frequency points by using the brightline control with the MARKER key. When this key is pressed a marker will be left at the brightline position. Up to eight markers may be displayed on the screen at any time. Any individual marker may be removed by placing the brightline back over it and pressing MARKER again, alternatively all may be removed by using the secondary function, ERASE.

Place marker at brightline position, or remove existing marker if brightline is coincident with it.

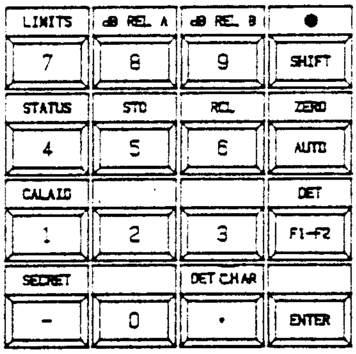


Remove all markers

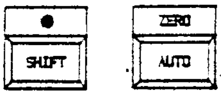
LOCAL key

The integral LED indicator in the LOCAL key monitors the state of the instrument under remote control. The LED off indicates remote control and the front panel keys (and brightline control) are inoperative apart from the LOCAL key. Providing the LOCAL LOCKOUT message has not been sent to the instrument, manual control can be regained by pressing LOCAL. This key has no effect when the instrument is already under manual control.

Miscellaneous functions



ZERO Key



The ZERO facility is used to set up the instrument´s signal channel after power-on and when changes in ambient temperature, or changes in the system occur.

The ZERO facility must only be used with **no incident RF** at the detector. If a ZERO is attempted with RF power applied to the detectors (and this cannot be completely nulled out) an error message will be displayed and all subsequent measurements will be affected.

When a channel has been successfully ZEROED, the message **Ready** will be displayed next to the channel identification. If no Probe is connected or the channel fails to ZERO, the messages **No Probe** or **Fail** will be displayed.

e.g. Probe on Channel A, No probe on Channel B, RF power on Channel R.

Autozero:

A **Ready**
B **No Probe**
R **Fail**

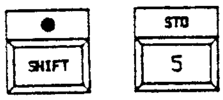
If a situation other than all channels being ´Ready´ occurs the message desribing the ZERO operation will be left displayed. No error is produced for a "No Probe" condition, but ** Error 42 ** message will be produced for a "Fail". A channel which has been successfully ZEROED will display a Power level, when averaged, between -55 and -61 dBm.

Note ...

The ZERO operation also sets up internal calibration which affects 10 dB range overlaps. Consequently if the ZERO operation occurs with RF power present these ranges covering all power levels will also be affected. However, if the ZERO drifts due to temperature changes of system effects, the inaccuracy introduced is greatest at low power levels. Before measurments are made at low power levels, a ZERO operation should be repeated with the RF turned off.

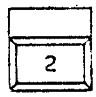
STO and RCL keys

Up to nine complete instrument states may be saved for recall later. To save an instrument setting press the SHIFT and STO keys.



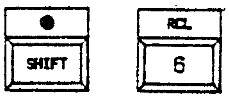
Prompt

Store Settings



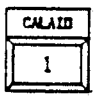
With the **Store Settings** prompt displayed the appropriate operating Store Number (1-9) should be selected. The following parameters are stored:

Limits and limit checking status.
DATUM and RANGE(s)
F1, F2, START and STOP
Sweep Speed
Channels and Mode including dB Rel values
Markers
Temperature correction ON/OFF
To recall one of these stores use RCL



Prompt

Recall Settings



The parameters in Store 1 are re-entered into the instrument and the STATUS is displayed for confirmation of the current state of the instrument. If nothing has been entered into given store and an attempt is made to recall data from it the *** Error 03 *** message will be displayed. It is useful to record the contents of each store on a worksheet. A sample worksheet is shown in Fig. 3-6.

Note ...

The contents of channel (display) memories are **not** stored.
Use STORE for this.

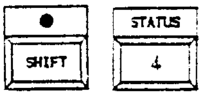
6500 AMPLITUDE ANALYSER - INSTRUMENT SETTINGS WORKSHEET

PARAMETER	STORE 1	STORE 2	STORE 3	STORE 4	STORE 5	STORE 6	STORE 7	STORE 8	STORE 9
F1 FREQUENCY									
F2 FREQUENCY									
START FREQUENCY									
STOP FREQUENCY									
SWEEP SPEED									
CHANNEL									
DATUM (A)									
RANGE (A)									
DATUM (B)									
RANGE (B)									
DATUM (R)									
RANGE (R)									
-R									
SUB M (A/B/R)									
dB REL (A/B)									
dB REL REF (A)									
dB REL REF (B)									
UNITS									
AVERAGE ON/OFF									
LIMITS ON/OFF									
HIGH LIMIT (A)									
LOW LIMIT (A)									
HIGH LIMIT (B)									
LOW LIMIT (B)									
MARKER 1									
MARKER 2									
MARKER 3									
MARKER 4									
MARKER 5									
MARKER 6									
MARKER 7									
MARKER 8									
TEMP. CORRn.ON/OFF									

Fig. 3-6 Sample work sheet

STATUS key

The current status of the instrument is displayed on the screen using the SHIFT and STATUS keys. Information is then provided about those parameters of the instrument which are not normally displayed.



Displays instrument status
An example is shown below.

6500 Status

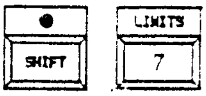
Channel Limits (Disabled)

A(High) +99.00	A(Low) -99.00
B(High) +99.00	B(Low) -99.00
dB Rel A 0.00	F1 0.01
dB Rel B 0.00	F2 18.00

GPIB Address:	8	
Detectors (ABR):	111	(Indicates detector types. See DET)
Temperature Correction:	On	

LIMITS key

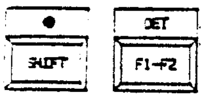
LIMITS is a toggle action key and is used in conjunction with the SHIFT key to either enable or disable the limits checking facility. Checking the operating limits takes approximately 10 ms. Consequently, disabling the facility will provide slightly faster sweep speeds. An "L" is displayed above the amplitude scale(s) on the upper left screen when the facility is enabled.



Enable/Disable limit checking facility.
Limit values not affected.

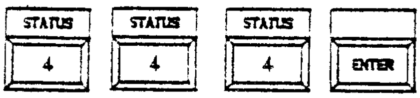
DET key

When an detector other than the basic 6511/12 type (0.01 - 18 GHz) is to be used, appropriate temperature and square law correction needs to be applied to that detector´s range. For the 6514 detector, the correction figures are stored in the 6500´s memory and these can be applied by selecting ´4´ for the appropriate channel(s) on selection of the DET key:



Prompt

Enter Detectors (ABR)

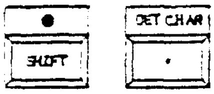


Similarly, ´1´ corresponds to the 6511/12 detector. If your instrument contains firmware Issue 7, the characteristics of the 6513 detector are stored in the instrument and can be applied by selecting ´3´. If your instrument contains firmware Issue 6, the 6513 correction figures will need to be entered via the DET CHAR key. See 6513 Instruction Manual for details.

If detector ´0´ is specified for any channel, square law correction and temperature compensation is disabled on that channel, so that the displayed amplitude has a square-law relationship to the actual amplitude, and is temperature dependent. The user can then make his own allowances for square law deviation and temperature errors. At power-on 6511/12 type detectors will always be selected for all three channels A,B and R.

The characteristics of non-MI detectors should be entered using DET CHAR.

DET CHAR key



The SHIFT and DET CHAR keys are used to enter the characteristics of up to three non-MI detectors. On selection the following table is displayed:

Enter Value:

Detector		Sensitivity Adjustment	Correction Start
7	>	0.00 dB	0.00 dBm
8		0.00 dB	0.00 dBm
9		0.00 dB	0.00 dBm

For each of the three "user programmable" detectors, 7, 8 and 9, there are two characterisation parameters:

(1) The "sensitivity adjustment" is a simple constant offset added to the detector's power reading. For example, the values automatically selected for the 6511 and 6514 are 0 dB and +3.9 dB respectively.

(2) The "correction start" is the power level at which square law correction begins to take effect. Correction start values automatically selected for the 6511 and 6514 are -27.0 dBm and -24.86 dBm respectively.

The method for establishing the values for non-MI detectors is given in Appendix A. Note that values must be obtained for each individual detector, not just for a particular type.

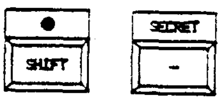
Values of sensitivity adjustment and correction factor may be entered into the table for each detector. The cursor > indicates the value which is currently enabled to be changed. Numeric values may be entered in the range -99.9 to +99.9 (dB/dBm), terminated by [ENTER]. If you press [ENTER] without numeric entry, the cursor steps to the next entry non-destructively.

When changes to the table are complete, press [NORMAL].

To use any of the "user programmable" detectors, use [SHIFT][DET] and select as described in the previous section.

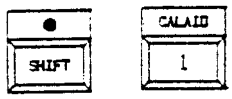
SECRET key

To remove the frequency scaling information, press SHIFT and SECRET keys. This is for use when frequency bands being used should not be generally displayed or are irrelevant. Usually used for photography/plotting. This function has a toggle action.



Remove/Restore frequency related information.

CALAID key



SHIFT and CALAID keys are used in the factory when initially setting up the instrument signal channel and for later re-calibration. It can also be used as a confidence check by the user.

The dispay removes the graticule and instead shows a measurement of power on the selected channel, and identifies which range(s) the instrument is using for the measurement as shown below. The columns R0, R1 and R2 show the appropriate states of the internal digital lines which select the ranges.

```
CALIBRATION AID

KEYS:0   CYCLE, 1-6  HOLD RANGE
     7-9 SELECT CHANNEL A,B,R

  TEMPERATURE SENSOR:    - 2.87

  RANGE          R0 R1 R2     POWER

1 - 1  - +16     1  0  0     +12.53
2 -15  - - 1     1  0  1
3 -25  - -15     0  0  0
4 -35  - -25     0  0  1
5 -45  - -35     0  1  0
6 -55  - -45     0  1  1

CHANNEL = A
```

Fig. 3-7 Calibration aid display

When in CALAID the Keys 0-9, SHIFT and SECRET have different functions:

0	An attempt is made to make a measurement on each of 6 ranges and readings which the instrument considers valid are displayed. This continues cyclically.
1 - 6	Holds range 1 - 6 (indicated by flashing "H" adjacent to selected range). Only when valid measurements are made on the held range will they be displayed.
7,8,9	Select which channel measurement is to be made on; A, B or R.
SHIFT	Select Temperature Correction ON/OFF (toggle action).
SECRET	If selected, the readings from the Temperature sensor are displayed, otherwise OFF will be displayed.

To check the integrity of the signal channel, adjust the RF power to a level where a reading is obtained on two adjacent ranges. The readings should be the same. The bar on the right will indicate any difference between the two.

Note ...

(1) A valid ZERO operation must have been performed.

(2) The bar should settle to the same level as the horizontal line on the centre; to reset the bar, reselect the channel.

(3) The setting of LINE and HISTOGRAM for the A or B channels may be disturbed after using CALAID.

The temperature correction facility makes allowances for variations in detector characteristics at different temperatures. A reading from the sensor is displayed for each Channel in CALAID if for any reason this is not required it can be switched out. The correction applied is insignificant in the temperature range 19-27 ^{0}C.

Chapter 3-2

APPLICATIONS

Introduction

The concept of swept frequency response testing is well established as a measurement technique. The versatility of 6500 enables a wide variety of microwave measurements to be made, without recourse to "pencilled" reference marks and without the need to establish reference offsets in dB ratio loss/gain measurements; in fact 6500 measures and displays absolute power. In addition the display provides all the information necessary to identify frequency, amplitude, out of limit operation, etc for the particular measurement.

The display, using on-screen graphics and the unique PLOT facility enables easy interpretation and recording of results.

Measurements that can be made using 6500 fall into 5 main categories:

Absolute power vs. Frequency
Transmission loss or gain vs. Frequency
Return loss vs. Frequency
Power output or gain vs. Power input\
Comparison or ratio measurements

The 6500 provides a ramp output voltage which is used to tune an RF source requiring either a fixed 0 - 10 V input or a variable 0 - 20 V input. Some RF sources may need adaptors to access this external drive (e.g. 8620C series sweepers from Hewlett Packard). Others may need minor changes to enable the external drive (e.g.6600 series Sweepers from Wiltron require the top cover to be removed and the EXT SWP switch turned on). In case of doubt refer to RF source manufacturer's instructions.

On multiband sweepers it may be necessary to use the SYNC input to 6500 to create a pause in the sweep ramp to allow for the time delay as oscillators covering different parts of the band are switched in and out. If this is not done, small break lines may appear in the 6500 display at band switch points. Ensure that any amplitude modulation (e.g. 1 kHz) is switched off.

Initialization of sweeper

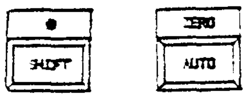
Initialization of the system is common to all measurements with 6500. Two main steps are involved:

i) Zeroing of the detectors.

ii) Alignment of frequency coverage with 6500 display.

Zeroing

Zeroing must be performed with the detectors connected to the instrument and the RF source turned off.

Press 

6500 holds up the sweep while the build up of DC voltages in the probes and front end ciruitry are nulled. The display shows when this operation is completed. Note that the Autozero Status Message is automatically erased at the end of the ZERO operation if all three channels zero satisfactorily. If the result is not as shown, refer to Chap. 3-1, "Zero key".

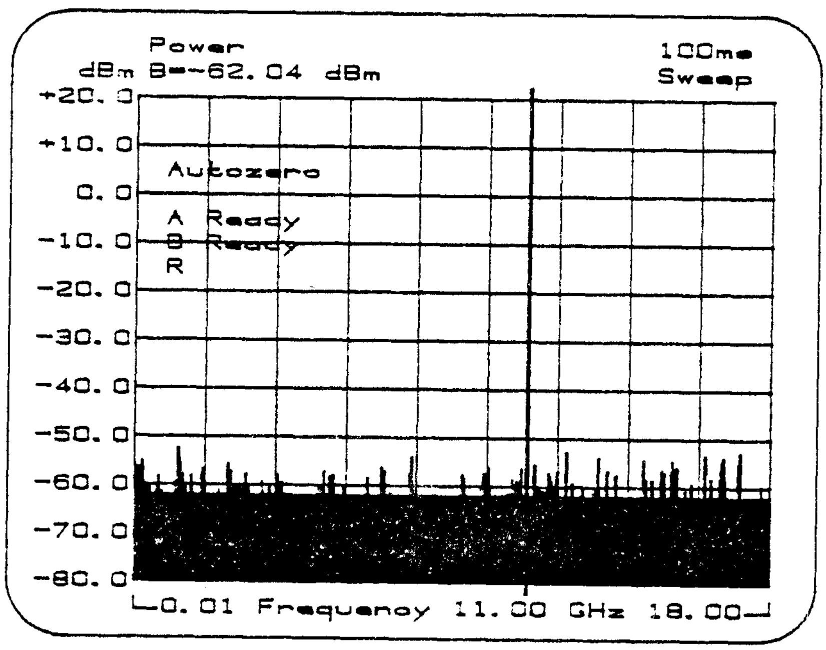
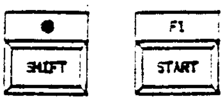


Fig. 3-8 Auto zero status message.

Alignment of sweeper frequency coverage with 6500 display

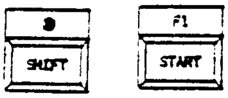
For sweepers driven from the 6500's 0-10 V ramp, frequency alignment is achieved as follows:

Set F1

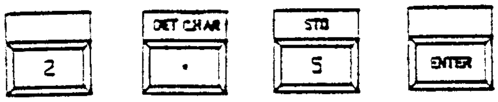


The 6500's ramp will be driven to 0 V and thus the sweeper frequency will be a minimum. Measure this frequency using a counter and enter it into the 6500. For example, to set up and enter F1 of 2.5 GHz the sequence is:

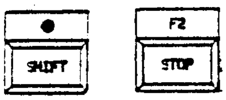
Prompt



Set Sweeper F1

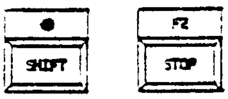


Set F2

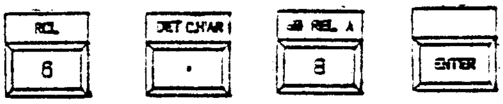


The 6500's ramp will be driven to 10 V and thus the sweeper frequency will be a maximum. Measure this frequency using a counter and enter it into the 6500. For example, to set up and enter F2 of 6.8 GHz the sequence is:

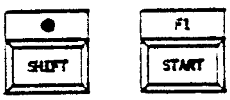
Prompt



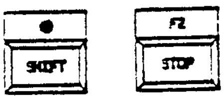
Set Sweeper F2



For sweepers which require a drive voltage other than 0-10 V but within the range 0-20 V, the 0-20 V ramp output is used. Before entering F1 and F2, the specified minimum and maximum voltages for the sweepers drive ramp must be set up as follows:



The ramp will be driven to the current minimum setting. Monitor the voltage across the 0-20 V output connector and adjust the OFFSET screwdriver control for the specified minimum drive voltage of the sweeper.



The ramp is driven to the current maximum setting. Again monitor the voltage across the 0-20 V output and use the C (coarse) and F (fine) screwdriver controls to adjust for the specified maximum drive voltage of the sweeper.

With the limiting drive voltages correctly set, the minimum and maximum sweeper frequencies can be set up, measured and entered as for the 0-10 V ramp.

Note ...

In the following procedures it is assumed that zeroing and frequency alignment have been carried out.

Absolute power measurements

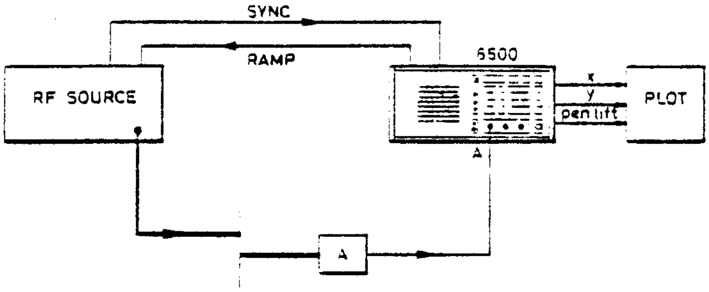
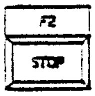


Fig. 3-9 Absolute power measurements, interconnecting diagram

6500 will display the absolute power output of the RF source. The maximum and minimum values can be read using the BRIGHLINE controls and the variation in power easily noted. Particular areas of interest in the swept power performance can be examined by using the BRIGHTLINE and



keys to change the displayed frequency range. The 6500 will display the power directly in mW on a scale 0 - 50 mW by depressing

key. The set up could also be used for checking the variation in power of solid state microwave oscillators such as varactor tuned Gunn and FET Oscillators using a linearizer if necessary. However the linearity of the frequency display would be no better than the linearity of tuning of the oscillator.

Insertion loss/gain measurements

The arrangement used for the absolute power measurement (Fig. 3-9) could be used to measure the insertion loss or gain of a device. The method would be to first connect the detector directly to the sweeper to obtain the characteristic trace of the sweeper in the frequency range of interest. This response would be stored to memory and the device under test (D.U.T.) inserted between detector and sweeper. If the stored sweeper response is now subtracted from the live display (using the SUB M key) it might be assumed that the trace obtained is a true representation of the response of the D.U.T. This assumption is not always correct, however, since:

(1) Sweeper output may vary with time.
(2) Sweeper output may vary with load.

To overcome this problem a reference channel (Channel R) is provided, which allows any variation in the output of the sweeper to be taken into account in the display of insertion loss/gain. This arrangement is shown in Fig. 3-10.

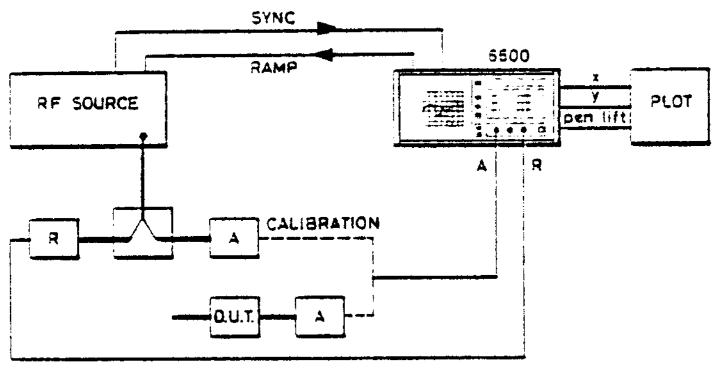


Fig. 3-10 Insertion loss/gain measurement, interconnecting diagram.

A power splitter is connected to the sweeper output wiht the reference channel (R) detector connected to one arm of the splitter and the measurement channel detector connected to the other arm.

This arrangement reduces the maximum displayed dynamic range by 6 dB, due to the loss in the splitter. If this is unacceptable, a directional coupler may be preferred. Another reason for preferring high directivity couplers is that they have better isolation characteristics than power splitters, which means that there is less chance of reflected signals from channnel R giving rise to errors on channel A.

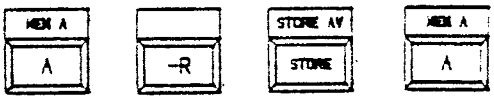
The measurement method is to first perform a calibration run of A-R and store this trace to memory A, then connect the D.U.T. and display the live A-R with memory A subtracted.

The technique still needs to be used with some caution since RF source harmonics will add to the power measured by the detectors and could (depending on the phase and on the characteristics of the device under test) give significant errors. RF source harmonics should be at least 40 dB down on the carrier level. The accuracy of the 6500 with 6510 series detectors is highest in the region of 0 dBm, and although the 6510 series detectors' square law deviation is corrected by the 6500, the errors increase as incident power increases. Hence measurements should ideally be made with incident power levels between +10 and -40 dBm. If sweeper harmonics are higher than -40 dBc, a low pass filter should be included in the output circuit, though this may limit useful measurements to octave band frequency ranges. To preserve a good source match a padding attenuator may be needed between the filter and the power splitter/coupler. The coupler should be of high directivity, again to provide a good source match.

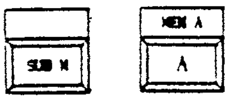
The error effect of RF source harmonics is tabulated in the Marconi Instruments publication "Microwave Datamate", which contains other useful information on microwave measurements.

The 6500's keyboard control allows the transmission loss/gain measurement to be made very rapidly. With detectors and any adaptors connected to the two arms of the power splitter or coupler select the following keys:

Without device under test:



Normalize display :



Insert device under test. Use AUTO if required to obtain best fit of the trace on the screen.

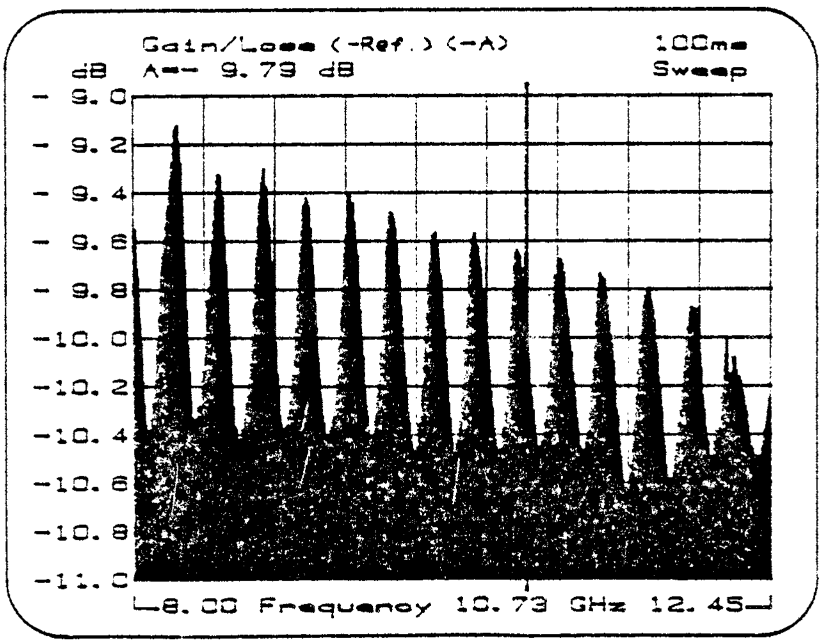


Fig. 3-11 Insertion loss measurement display

Measurement of return loss

Return loss or VSWR of a device may be measured using a high directivity coupler or bridge to provide a sample of the reflected power. The use of the reference channel, the need for low source harmonics and the need for a good source match are equally applicable for the accuracy of this measurement.

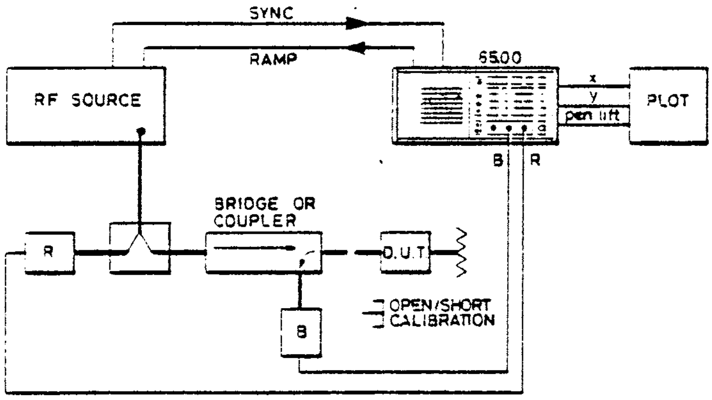


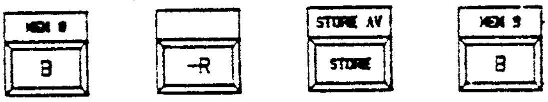
Fig. 3-12 Return loss measurements, interconnecting diagram

To provide a calibration for return loss or VSWR measurements the average value of reflections from an open circuit and a short circuit over the frequency band of interest is stored in memory B.

The Reference channel, as before, is subtracted from each display to remove variation of the RF source. When the unit under test is connected to the test port the resultant return loss is displayed by subtracting R and subtracting memory B. This return loss may be viewed directly as a VSWR on a scale up to 3:1 by pressing the UNITS key.

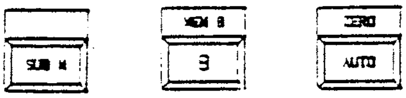
If the device under test is a one port device the above procedure is adequate bearing in mind the sources of error due to source match, detector variations and 6500 channel accuracy. However if the unit under test is a multiport device, the remaining ports should be properly terminated.

A microwave bridge usually has an insertion loss of about 6 dB and this may limit the effective dynamic range, particularly since the power handling may be limited. A coax wideband coupler, however, generally has a narrower frequency range with reduced insertion loss and higher power handling capability. With open circuit termination to bridge or coupler, store the response in memory B by selecting the following keys:



Replace open circuit by short circuit and then select SHIFT, STORE AV, and B channel keys:-

This stores the average of the open and short circuit reflections in Memory B without the effect of sweeper variations. Insert device under tests, properly terminated if necessary, and select the following keys:-



The display now shows the return loss of the device in dB.

To convert to VSWR press the UNITS key.

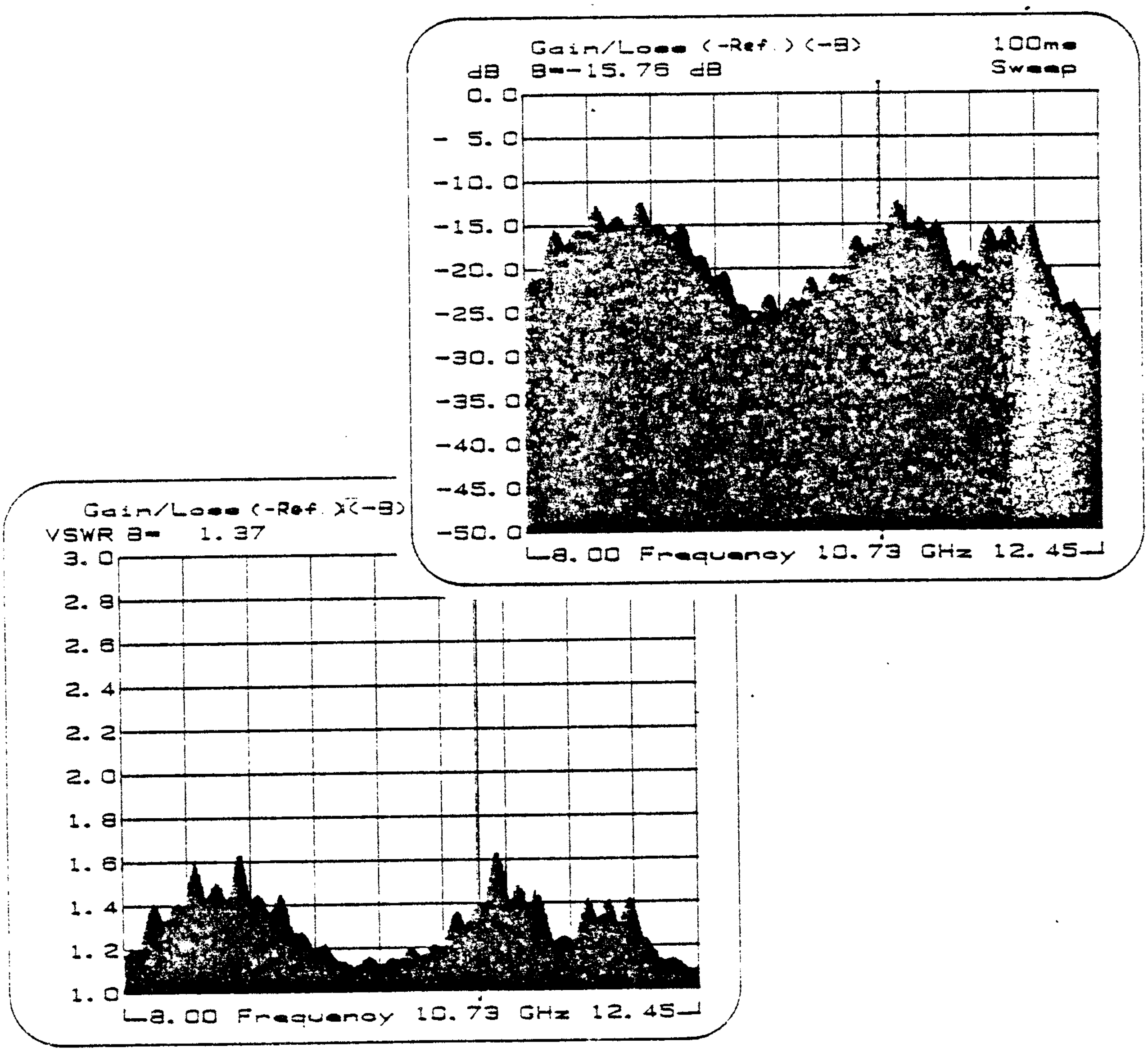


Fig. 3-13 Return loss measurement display

Simultaneous return loss and transmission loss measurement

The procedure follows that for Return loss in that the channel A detector senses the transmitted signal, channel B the return loss signal, and channel R is used for reference to normalize the response. Open and short circuit calibration data is stored in Memory B and subtracted from the display on channel B once the unit under test is inserted e.g. Connect detector A to measurement plane.

Measure power at A subtracting reference channel and store in Memory A

MEM A		STORE AV	MEM A
A	-R	STORE	A

Remove detector A and follow procedure for open and short circuit calibration.

Open circuit:

MEM B		STORE AV	MEM B
B	-R	STORE	B

Short circuit:

●	STORE AV	MEM B
SHIFT	STORE	B

Remove the short circuit and insert the device under test:

For Return Loss:

MEM B			MEM B	ZERO
B	-R	SUB M	B	AUTO

For Transmission Loss:

MEM A			MEM A	ZERO
A	-R	SUB M	A	AUTO

Both may be viewed by pressing the following keys:-

			MEM B		MEM A	ZERO
A&B	-R	SUB M	B	SUB M	A	AUTO

The results are shown illustrated in Fig. 3-14.

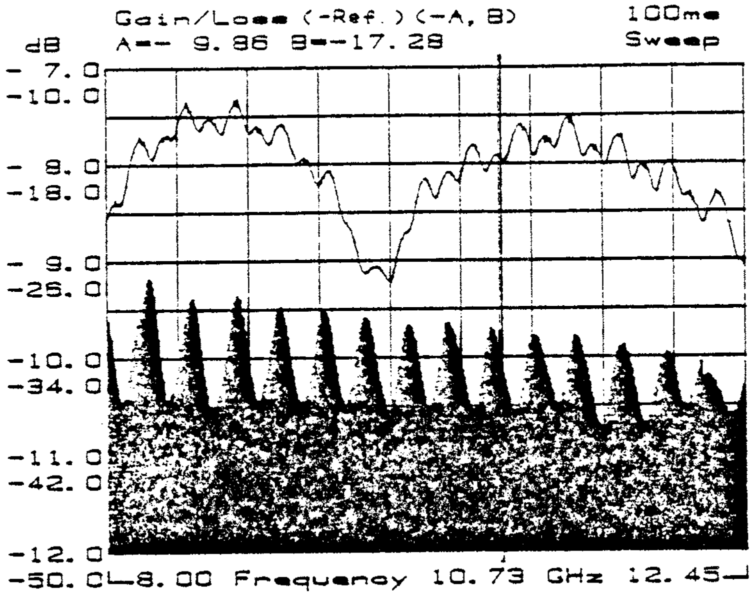


Fig. 3-14 Simultaneous return loss and transmission loss display

Waveguide measurements

Using similar high directivity coupler (>40 dB), return loss and transmission loss measurements may be made in waveguide systems using the arrangement shown in Fig. 3-15. The 6511 or 6512 detectors are coupled to the system through coax to waveguide transformers.

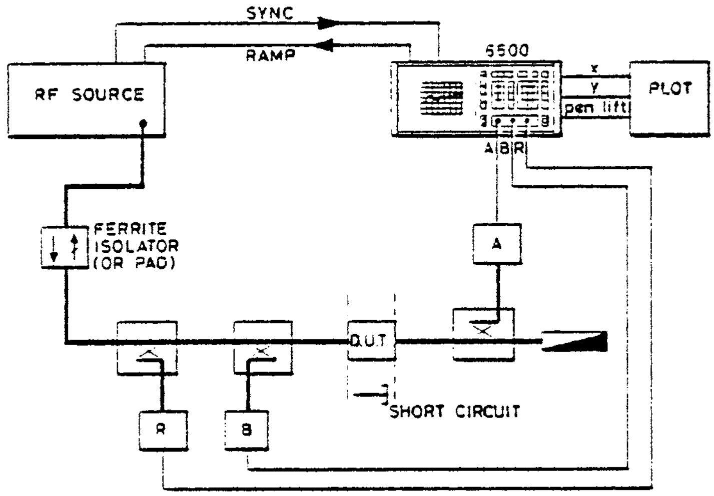


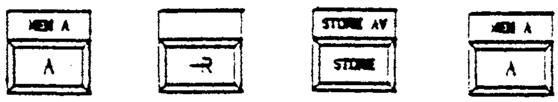
Fig. 3-15 Waveguide measurements, interconnecting diagram

Calibration is made using a waveguide short circuit. The device under test is then inserted at the measurement port and the display shows return loss when the reflection due to the short circuit is subtracted.

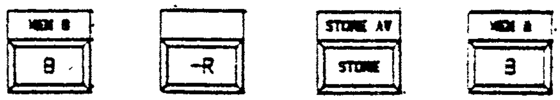
The signal transmitted through the device under test is sensed by detector A which is connected either directly to the device via a transformer or through a 3rd waveguide coupler. This improves the match seen by the test device but is not necessary from the point of compensating for coupler variation as 6500 memory capability can calibrate the through line. Low VSWR coax to waveguide transformers must be used to reduce measurement uncertainty.

Using the arrangement shown in Fig. 3-15:

(1) Establish reference data for channel A by connecting to measurement port select:-



(2) Establish reference data for reflection on channel B by substituting short circuit at measurement port.



(3) Remove short circuit and insert the device under test. Return loss may then be measured by subtracting memory B from B-R and transmission loss measured by subtracting memory A from A-R.

Amplifier 1 dB compression point measurements

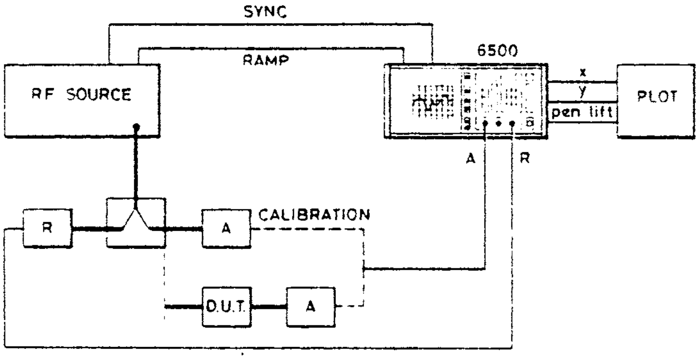
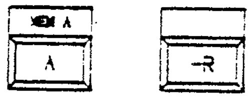
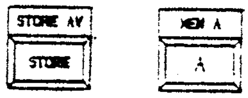


Fig. 3-16 Amplifier 1 dB compression point measurements

This technique uses a ratio between input and output powers followed by a relative output power measurement also including frequency normalization.

(1) With the equipment set up as shown in Fig. 3-16 connect channel A detector directly to the power splitter and ensure that the amplifier is operating in its linear region.

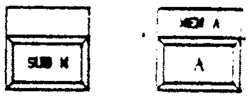
(2) Carry out a ratio measurement selecting A and -R: 

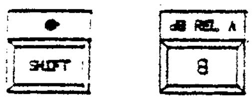
(3) Normalize the frequency response by selecting: 

(4) Insert the amplifier (D.U.T.) between the channel A detector and the power splitter.

Note...

If the amplifier has an output level greater than +16 dBm a suitable attenuator pad should be inserted before the detector.

(5) Measure the amplifier gain thus: 

(6) Select a reference point on the display with the brightline control and reference this point to 00.00 dB by selecting: 

(7) Set DATUM to +1 dB, set RANGE to 1 dB/div. Increase the RF source level until the response at the reference point falls by 1 dB, this indicates the 1 dB compression point.

(8) The actual amplifier output power at this frequency can be measured by selecting channel A  and reading power at the brightline frequency.

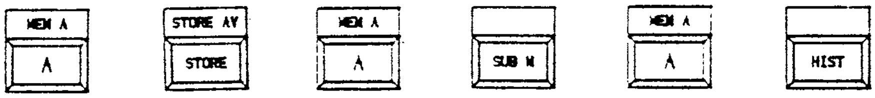
Note...

If an attenuator was included before channel A detector, its value (at the brightline frequency chosen as reference) must be added to the power measured.

Comparison of device performance against a stored reference

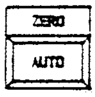
There are occasions when the gain or loss of an unknown or test device such as a filter or amplifier needs to be compared with that of a reference device. One technique is as follows (use of channel R is omitted for clarity):

(1) With detector A connected to the RF source select:-



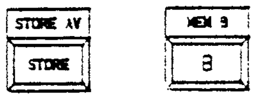
This serves as a calibration and normalization procedure.

(2) Insert "standard" device between RF source and detector A and select

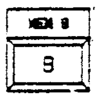


to display response of "standard" device.

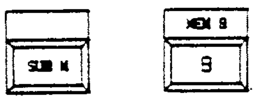
(3) This "standard" response is now stored in memory B by selecting



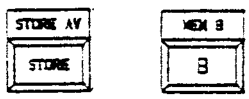
(4) Without detector B connected to channel B input select:-



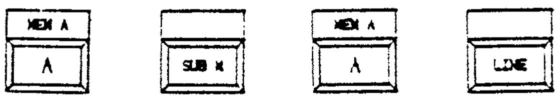
The display shows B channel at its lowest level without the noise contribution of detector B. Select:-



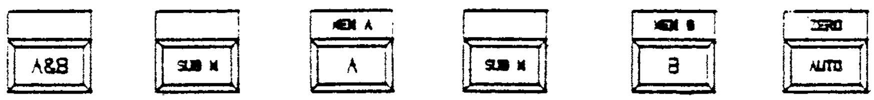
This subtracts the "standard" trace from the low level in B and it is then re-written into memory B by selecting:-



(5) The test device is now substituted for the "standard" device and displayed as a line by selecting:-



(6) Finally to compare and display the stored "reference" as a histogram and the current test performance as a line in a normalized form select:-



Measurements of gain/loss tracking between similar devices

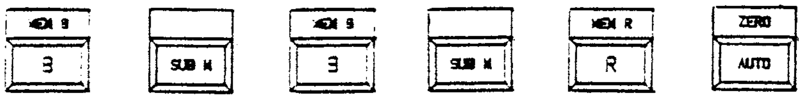
This technique can be used to examine the differential gain or loss between for example matched amplifiers or attenuators. After initialization the procedure is a follows:

(1) Normalize for systems errors by connecting A and B detectors to both arms of a power splitter fed from the RF source and select:

and

(2) The two test devices are then inserted in the lines between the splitter arms and the detectors. One device (e.g. that on Channel A) is then normalized and stored in memory R by selecting:

(3) The other channel is now normalized and the performance of the other device subtracted by selecting:



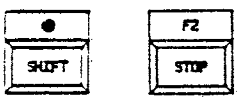
This display now shows the difference between the two devices.

Control of graticule lines

Vertical graticule lines may be re-instated at sweep widths less than 0.1GHz. Three methods of achieving this are shown in the following paragraphs.

Scaling factor method.

(1) Select SHIFT and F2 (F2 is selected to avoid ´error´ prompts when entering a number where F1 > F2)



Prompt

Set Sweeper F2

(2) Measure RF source output frequency with a frequency counter.

(3) Enter this value directly by the keyboard, keeping the resolution required, e.g. 52.47 MHz.

Normal entry :	0.05 GHz
x10 Resolution :	0.52 GHz
x100 Resolution :	5.24GHz
x1000 Resolution :	52.47 GHz

(4) Repeat the procedure for F1.

(5) Note that with F2-F1 difference greater than 0.1 GHz, vertical graticule lines will be present.

(6) The display readout must be scaled down by the factor chosen.

Counter method

(1) Select SHIFT and F1. Enter frequency information in the normal manner e.g. 50 MHz as 0.05 GHz.

[● / SHIFT] [F1 / START] Prompt **Set Sweeper F1** [DET CHAR / .] [0] [STO / 5] [ENTER]

(2) Select SHIFT and F2 (MHz) normally in GHz. Graticule lines may not now be present.

(3) To identify a frequency on the display, connect a frequency counter permanently to the RF source output. Then select FREEZE.

[FREEZE] The brightline control is now linked to the ramp output of the manual frequency control. At any point on the display the frequency may be read directly from the counter by varying the brighline control.

(4) If required up to eight markers can then be placed on the screen at frequencies of interest whilst in this mode by pressing the MARKER key.

[ERASE / MARKER] Select NORMAL to continue sweeping [SPEED / NORMAL]

Ten division graticule method.

(1) Select SHIFT and F1. Enter F1 as 0.0 GHz.

[● / SHIFT] [F1 / START] Prompt **Set Sweeper F1** [0] [ENTER]

(2) Select SHIFT and F2. Enter F2 as 100 GHz.

[● / SHIFT] [F2 / STOP] Prompt **Set Sweeper F2** [CAL AID / 1] [0] [0] [ENTER]

The display now divides into 10 equally spaced vertical graticules. Because the display shows 0 to 100 GHz frequency range, select SHIFT and SECRET to remove the erroneous frequency information

[● / SHIFT] [SECRET / -]

(3) To read frequency information from the display, connect a counter to the RF source output. Select SHIFT and FREEZE and the frequency at the brightline point con be read to the required resolution.

[● / SHIFT] [FREEZE] Select NORMAL to continue sweeping [SPEED / NORMAL]

Broadband frequency response using a frequency window

The following procedures define two methods of broadband frequency response measurements using a "fixed window" or Δf for examination of response slopes prior to gain equalization.

Sweep generator method.

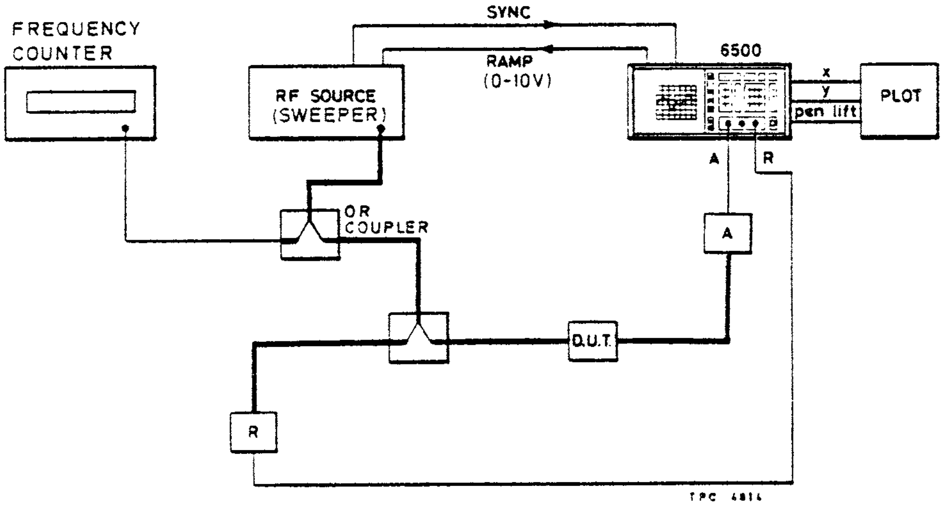


Fig. 3-17 Broadband measurements using a frequency window interconnecting diagram

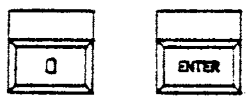
Connect up the equipment as shown in Fig. 3-17 and set the RF source to EXTERNAL operation, connect the 6500 0-10 V FIXED RAMP output to the EXT INPUT of the RF source and the frequency counter to one arm of the power divider or coupler.

(1) Set the RF source CW control to the lowest frequency of interest and select the Δf facility.

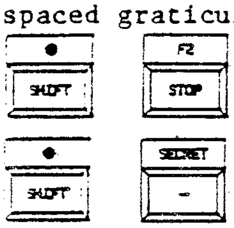
(2) Select SHIFT and F1 on the 6500, note the counter reading an adjust the CW control until the desired lowest frequency is displayed. Enter 0 on the keyboard.

Prompt

Set Sweeper F1

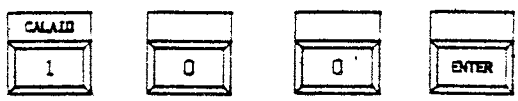


(3) Select SHIFT and F2 on the 6500, note the counter reading and adjust the RF source Δf control until the counter reads the incremental frequency shift required. Enter 100 on the keyboard and the equally spaced graticules are now generated



Prompt

Set Sweeper F2



Select SHIFT and SECRET to erase the frequency information written to the screen and the Δf sweep is now calibrated.

(4) With the measurement detector on channel A connected to the output of the system and the reference detector R, the ratio of the input to output can be displayed and measured on the 6500.

(5) The DATUM and RANGE may be reset to give values within the test specification or alternative AUTO RANGE may be used to optimize the DATUM and RANGE settings.

(6) By operation MAX and MIN keys, the amplitude values at these points can be measured and the difference in frequency slope measured.

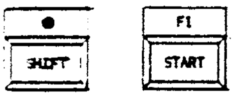
(7) To measure response slopes at any other window position, simply vary the CW control of the sweeper and the display will show the frequency response of the system passing through the "fixed window". Measurements are repeated as above.

Voltage tunable oscillator method

Connect up the equipment as shown in Fig. 3-17 substituting a voltage tunable oscillator (VTO) for the sweeper RF source. Select FM operation on the voltage tunable oscillators and connect the 0-20 V VARIABLE RAMP output to the external FM input of the VTO, (caution : check that maximum acceptable FM input level is not exceeded).

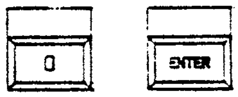
(1) Set the VTO control to the lowest frequency of interest using the frequency counter.

(2) Select SHIFT and F1 on the 6500. Note the frequency counter reading and enter 0 GHz on the keyboard.

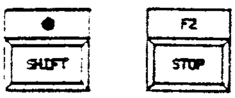


Prompt

Set Sweeper F1

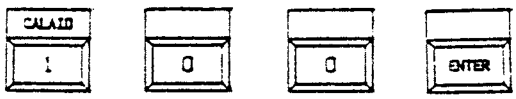


(3) Select SHIFT and F2 on the 6500. Adjust the VTO CW control to give the required incremental frequency shift as shown on the frequency counter and adjust COARSE (C) and FINE (F) RAMP, 6500 rear panel controls to give the desired incremental frequency display. Re-adjust VTO, C and F controls and also if necessary the 6500 rear panel OFF SET control to maintain the required F1 frequency position. On completing the adjustments enter 100 on the keyboard. Ten equally spaced graticules will be generated



Prompt

Set Sweeper F2



(4) Select SHIFT and SECRET to erase the erroneous frequency information written to the screen. The "fixed window" or Δ is now calibrated and measurements outlined in the "Ten division graticule method" may be carried out.

NOTES

Appendix A

CHARACTERIZATION OF NON-MARCONI INSTRUMENTS DETECTORS

Detectors from manufacturers other than Marconi Instruments may be used if the appropriate correction figures are entered into the 6500 via the [DET CHAR] key. The method described matches the response of an ´unknown´ detector to that of a 6511 by adjustment of the correction factor and sensitivity factor.

Equipment required

6500
6511
Power splitter specified for operation at 2 GHz
Microwave sweeper capable of producing a levelled power sweep from -15 dBm to at least +10 dBm at 2 GHz (MI 6300 series sweeper recommended).
Connecting cables (precision N-type and BNC)

Arrangement

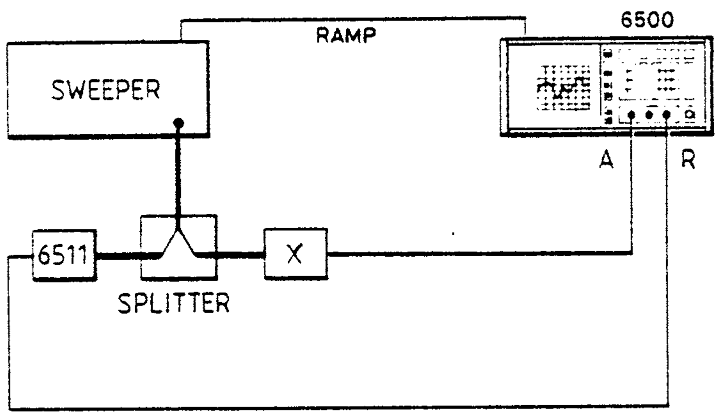


Fig. A-1 Arrangement for characterization of non-MI detectors

Method

(1) With RF power swiched off, connect the equipment as shown in Fig. A-1.

(2) Select [SHIFT][DET] on the 6500. The prompt **Enter detectors (ABR)** appears. Press [7][1][1][ENTER]to assign:
No correction (initially) to the unknown detector on Channel A,
6511 correction to Channel B (unused) and
6511 correction to the 6511 detector on Channel R.

(3) Select [SHIFT][ZERO] to zero the two detectors.

(4) On the sweeper set a continuous frequency of 2 GHz and a power sweep from -15 dBm to +15 dBm (or maximum levelled power if lower).

(5) Switch RF on. Select [A][-R] on the 6500. A trace of the form shown in Fig. A-2 should be obtained.

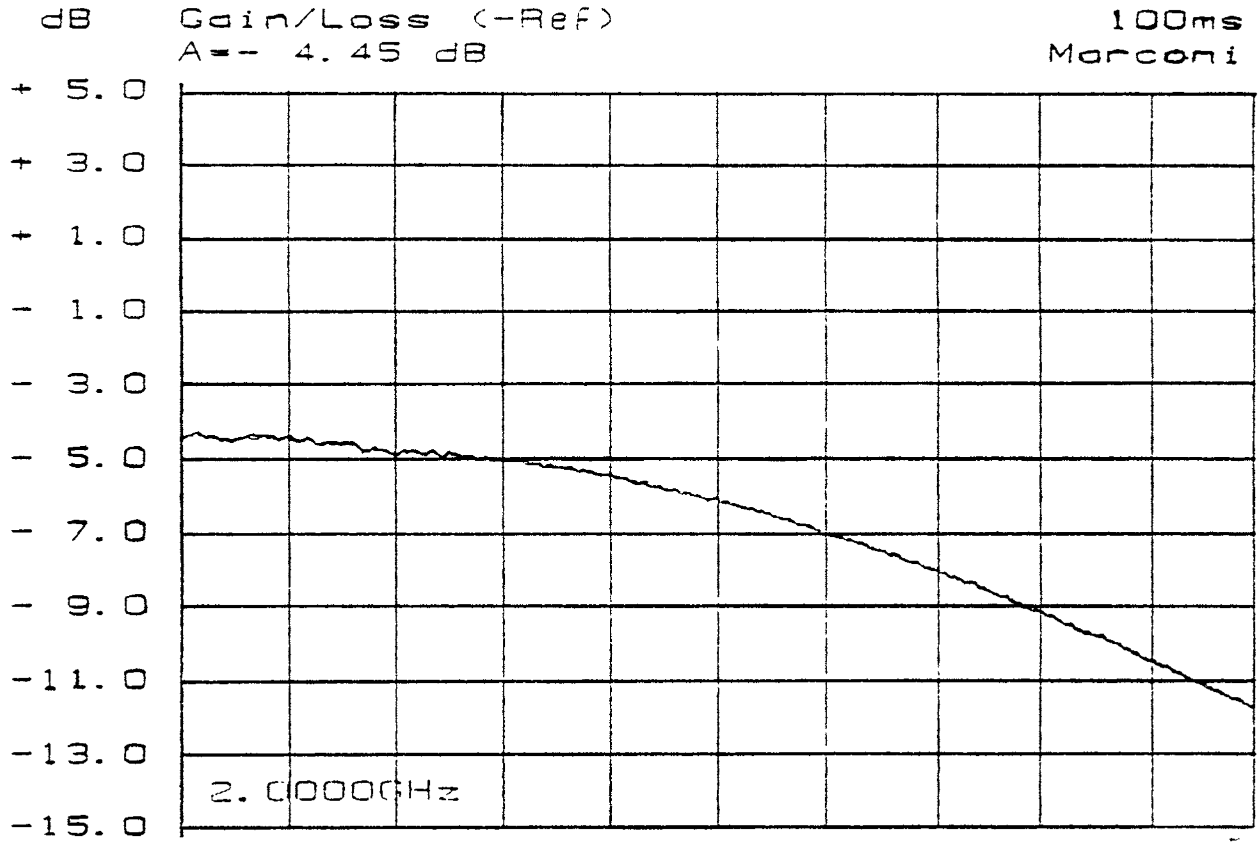


Fig. A-2 Response of unknown detector with respect to 6511

The trace represents the difference in response of the unknown detector with respect to the 6511. To match the responses, the correction and sensitivity factors for the unknown detector (currently zero) need to be adjusted so that a horizontal line at 0 dB is obtained.

(6) Select [SHIFT] [DET CHAR]. Starting with a value of -27 dBm, adjust the correction factor for sensor 7 to bring the trace to the horizontal. After each new figure has been entered press [NORMAL] to view the effect on the trace. Note that increasing the **negative** value of correction factor causes the trace to bend **upwards**, and vice versa.

(7) When a horizontal line is obtained, the sensitivity factor should be adjusted to shift the line to the 0 dB position. Alternatively, if a 0 dBm reference signal is used (available in MI's 6950 and 6960 RF Power Meters) absolute (rather than relative) accuracy at 0 dBm can be obtained by connecting the unknown detector directly to the power reference, selecting [A], and adjusting sensitivity factor to give a horizontal trace at 0 dBm. Note that increasing the **positive** value of sensitivity factor shifts the trace **upwards**, and vice versa.

With the sensitivity and correction factors correctly entered, the sensor can be used on any channel by selecting [DET] and [7] appropriately.

Correction figures for up to 3 non-Marconi Instruments detectors (7, 8 and 9) may be entered. When using a Marconi Instruments 6310 series sweeper the correction figures are held in non-volatile store

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AUTOMATIC AMPLITUDE ANALYSER
6500
GPIB OPERATION

IEEE 488-1978   SH1,AH1,T5,L4,SR1,RL1,DC1,E1

Part No. 46881-558S
Print Code : D-5/87, MI 1.0c

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INTRODUCTION

General purpose interface bus (IEEE-488/IEC 625)

1. The 6500 GPIB interface allows the instrument to be connected to a GPIB controller and other GPIB compatible devices. This manual describes the GPIB commands implemented on 6500 and, where appropriate, gives examples of their use. Programming examples are given for use on Hewlett Packard HP85 and Series 200 controllers. Further information on the general provisions of the IEEE-488 standard and its implementation may be found in the Marconi Instruments GPIB Manual (Part No. H 54811-010P). Familiarity with 6500 LOCAL operation is assumed. See operating manual H 6500, Vol. 1 for details.

Note...

The information contained in this operating manual pertains to 6500 firmware issue 5. See Appendix A for details of compatibility with pre-issue 5 versions.

INTERFACE FUNCTION CAPABILITIES

2. SH1 : Source Handshake - complete capability. The source handshake sequences the transmission of each data byte from the instrument over the bus data lines. The sequence is initiated when the function becomes active, and the purpose of the function is to synchronize the rate at which bytes become available to the rate at which accepting devices on the bus can receive the data.

3. AH1 : Acceptor Handshake - complete capability. The acceptor handshake sequences the reading of data bytes from the bus lines.

4. T5 : Talker Function - complete capability. The talker function provides the 6500 with the ability to send device dependent messages over the bus to other devices. Unless in TALK ONLY mode the ability to talk exists only when the instrument has been addressed as a talker. The TALK ONLY mode is provided on the 6500 to allow direct interfacing to an intelligent digital plotter.

5. L4 : Listener Function - no LISTEN ONLY function. The listener function provides a device with the ability to receive device dependent messages over the bus. The capability exists only when the device is addressed to listen by the controller.

6. SR1 : Service Request Function - complete capability. The service request function gives the 6500 the ability to interrupt the controller and request attention. The 6500 can be enabled to issue the interrupt on the occurrence of a number of a number of different events and returns a STATUS BYTE indicating the source of the interrupt when interrogated by the SERIAL POLL technique. PARALLEL POLLING is not supported.

7. RL1 : Remote/Local Function - complete capability. The remote/local function allows the 6500 to be controlled either locally by the front panel controls, or remotely by device dependent messages over the bus.

8. DC1 : Device Clear Function - complete capability. The device clear function is a general reset and may be given to all devices in the system (DCL - DEVICE CLEAR) or only to addressed devices (SDC - SELECTED DEVICE CLEAR). On receipt of DCL or SDC the 6500 performs a software reset, returning the instrument to its power-on state. The software reset includes the following actions :

SELF TEST
CLEAR ALL MEMORIES
SET DETECTOR ZERO AND NULL VOLTAGES TO NOMINAL VALUES
INITIALIZE ALL INSTRUMENT SETTINGS
READ GPIB ADDRESS SWITCH
RETURN 6500 TO LOCAL CONTROL

Note...

A self test failure may cause a GPIB interface error condition or suspend GPIB activity. The 6500 must be switched off to clear this condition.

9. E1 : Bus Driver Type. The GPIB driver devices fitted in the 6500 interface have open-collector, rather than tri-state outputs.

Chapter 2

INSTALLATION

CONTENTS

INSTALLATION PROCEDURE

1. The procedure described assumes that a GPIB interface is being installed in a 6500 which previously had none fitted. The interface may be installed as follows :

(1) Switch the instrument off and disconnect from power supply.

(2) Remove and discard the rectangular cover plate from the left-hand side of the rear panel. Also remove the instrument's bottom cover. Insert the cable and p.c.b. through the rear panel such that the GPIB connector is on the left-hand side. Using the two retaining screws from the cover plate, secure the GPIB assembly to the rear panel.

(3) Feed the interface cable through the cut-out in the bulkhead metalwork as shown in Fig. 1 and connect the interface plug to SK14 on the 6500 mother board, observing correct polarity.

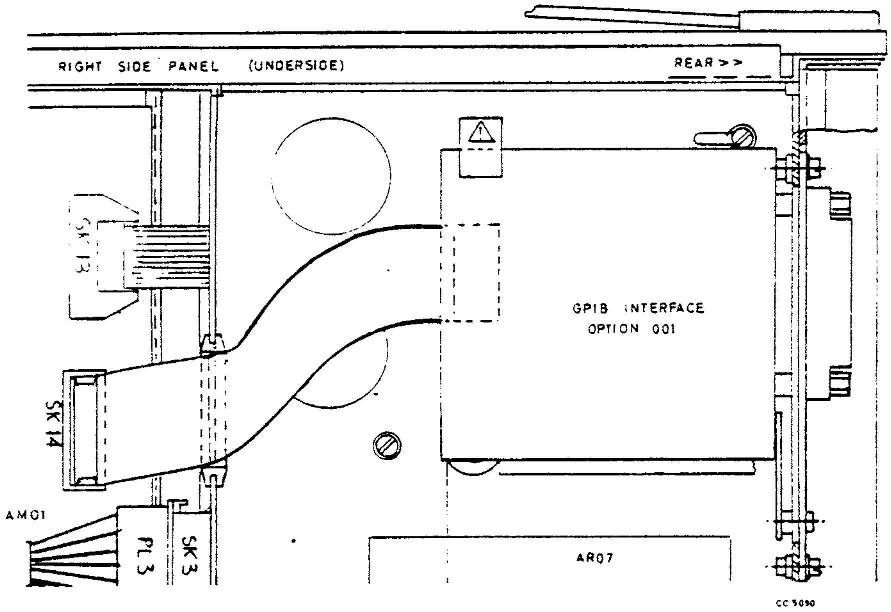


Fig. 1 Interface installation

(4) Add the two supplied self-adhesive labels to the rear panel identifying the GPIB connector and address switch as shown in Fig. 2.

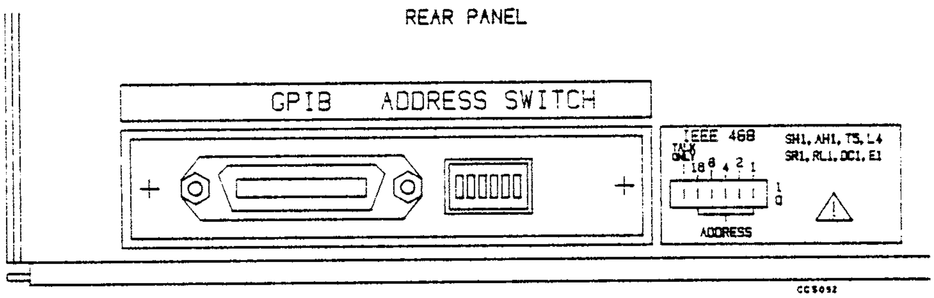


Fig. 2 Label positioning

(5) Replace the instrument's bottom cover.

The instrument is now ready for GPIB operation.

GPIB ADDRESS/TALK ONLY SELECTION

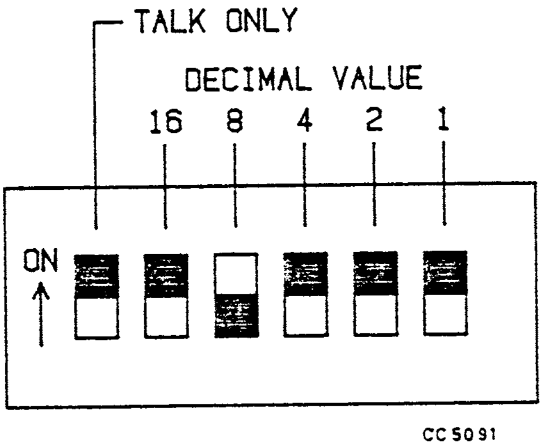


Fig. 3 Address switch configuration

2. The GPIB address switch is shown in Fig. 3. For normal operation the TALK ONLY switch should be off and the required address should be selected on the five address switch positions using the binary weighted decimal values shown. The interface is supplied pre-set to address 8. The normal valid address range is 0 to 30. Before changing the address check your controller manuals for reserved addresses.

3. TALK ONLY mode is activated by placing the TALK ONLY switch in the ON position. This mode is intended for use in a stand-alone configuration with a digital plotter. TALK ONLY must NOT be selected when the instrument is connected to a GPIB system governed by a controller.

4. Any change made to the GPIB address switch will only be recognized by 6500 after a power-on sequence.

Chapter 3

OPERATION

CONTENTS

Remote operation

1. On receipt of the Remote Enable (REN) signal from the GPIB the 6500 switches to remote operation, indicated by the LOCAL lamp being extinguished. No instrument settings are changed but all front panel keys except LOCAL are disabled and their functions come under GPIB control.

2. Unless inhibited by the Local Lockout (LLO) message the instrument can be returned to LOCAL control by pressing the LOCAL key or sending the Go To Local (GTL) or Interface Clear (IFC) messages or releasing the Remote Enable (REN) signal.

GPIB program codes

3. All valid GPIB program codes are listed in Table 1 and Table 2. Table 1 lists those codes which correspond directly to front panel key strokes, while Table 2 lists all others. Note that access to the secondary key functions is achieved by using the primary function code prefixed with 'SH'. 'SH' is treated by the instrument as a program code corresponding to the SHIFT key.

4. Program codes may be combined in a string without individual terminators, although spaces or commas may be included to improve clarity. These will be ignored by the instrument.

TABLE 1

PRIMARY KEY-STROKE COMMANDS

CA/B/R/C	Select channel A/B/R/A&B
SLR	Subtract Live Reference (-R)
STA/B/R/C	Store to memory A/B/R/A&B
SBA/B/R	Subtract memory A/B/R
U	Change measurement units
SD<n>E	Set screen datum dB(m)
SR<n>E	Set screen range dB(m)/division
SS<n>E	Set start frequency GHz
SP<n>E	Set stop frequency GHz
E	Enter (follows numeric data)
AR	Auto range
FW	Full width sweep (F1-F2)
DF<n>E	Sweep about brightline GHz
MX	Set brightline to max point
MN	Set brightline to min point
MK	Marker place/remove
N	Normal sweep mode
AV	Sweep averaging mode
FZ	Sweep freeze mode
H	Select histogram display
L	Select line display
P	Enter plot mode

SECONDARY KEY-STROKE COMMANDS (SH = SHIFT)

SHCA/B/R	Display memory A/B/R
SHSTA/B/R/C	Store average to mem A/B/R/A&B
SHSD<n>E	Set high limit dB(m)
SHSR<n>E	Set low limit dB(m)
SHSS<n>E	Set sweeper minimum (F1) GHz
SHSP<n>E	Set sweeper maximum (F2) GHz
SH1	Calibration aid
SH4	Display instrument status
SH5n	Store instrument settings
SH6n	Recall instrument settings
SH7	Enable/disable limit checking
SH8<n>E	Set dB relative (A)
SH9<n>E	Set dB relative (B)
SH-	Secret (blank frequency) mode
SHAR	Zero detectors
SHFWnnnE	Select detector types
SHMK	Remove all markers
SHNn	Set sweep speed
SH.<n>E....<n>E	Set detector correction figures (detectors 7,8,9) six entries in dB(m)

TABLE 2

BLOCK TRANSFER COMMANDS

RMA/B/R	Read ASCII from channel A/B/R
SHRMA/B/R	Read ASCII from memory A/B/R
WMA/B/R<a>	Write ASCII to channel A/B/R
SHWMA/B/R<a>	Write ASCII to memory A/B/R
RYA/B/R	Read BINARY from channel A/B/R
SHRYA/B/R	Read BINARY from memory A/B/R
WYA/B/R<b>	Write BINARY to channel A/B/R
SHWYA/B/R<b>	Write BINARY to memory A/B/R

BRIGHTLINE CONTROL/DATA TRANSFER COMMANDS

BR	Move brightline right
BL	Move brightline left
BP<i>E	Set brightline position
RP	Read brightline position
RA/B/R	Read brightline amplitude A/B/R
RF	Read brightline frequency
WD<n>E	Write brightline amplitude data

STATUS OUTPUT COMMANDS

RS	Read status string
RX	Read extended status string
RDA/B/R	Read display parameters A/B/R
RDF	Read frequency parameters
RMK	Read marker positions
RDM	Read delta marker value (power)

DIGITAL PLOTTER COMMANDS

DPA/B	Read HPGL string for trace A/B
DPG	Read HPGL string for graticule
DPL	Read HPGL string for labels

TEXT/KEYBOARD CONTROL COMMANDS

WTtitle$	Write title to top line of CRT
TX"text"	Write text to CRT
DA	Display alphanumerics only
RK	Read code of last key pressed
XK	Execute last key read by RK

MISCELLANEOUS COMMANDS

SQnnnnn	Set SRQ mask
SH2	Enter synthesizer mode
SH3	Step in synthesizer mode
RIn	Read instrument settings store
WIn	Write instrument settings store

DATA FORMAT CONVENTIONS USED ABOVE

n	Fixed field digit
<n>	Floating field data (NR2)
<i>	Floating field integer
<a>	ASCII block data (NR2 or NR3)
<b>	BINARY block data
"text"	Any number of valid ASCII bytes contained within quotes. Values 0-15 are used as control codes.

The E command terminates <n> and <i> data.

Data entry and terminators

5. Some program codes are acted upon immediately, while others require the addition of arguments to quantify their meaning. These codes fall into two groups; those requiring numeric data correctly terminated, and those requiring a single character argument with no terminator. Block transfers are a special case and are discussed separately.

6. Numeric data should conform to NR2 format as defined in IEEE 728-1982 and should be terminated with 'E'. This is treated by the 6500 as a program code for the ENTER key. This technique ensures complete compatibility with manual operation. The allowable range and resolution of the numeric data depends on the type of operation being performed.

7. Program codes requiring the 'E' terminator are :

SD	SET DATUM
SR	SET RANGE
SHSD	SET HIGH LIMIT
SHSR	SET LOW LIMIT
SS	SET START FREQUENCY
SP	SET STOP FREQUENCY
SHSS	SET SWEEPER MINIMUM
SHSP	SET SWEEPER MAXIMUM
DF	SET DELTA F SWEEP WIDTH
SH8	SET dB REL A
SH9	SET dB REL B
*SHFW	SET DETECTOR TYPES
*BP	SET BRIGHTLINE POSITION
WD	WRITE DATA
SH.	SET DETECTOR CHARACTERISTICS

* NR2 format is not used for these commands.

8. Program codes which require a single character argument are :

SH4	STORE INSTRUMENT SETTINGS
SH5	RECALL INSTRUMENT SETTINGS
SHN	SET SWEEP SPEED

Note...

The SQ command has a 5 digit argument which does not require the 'E' terminator.

Reading data from the 6500

9. When addressed to talk the 6500 can output data relating to various operating parameters. Some program codes are used to instruct the instrument which data is required. The data will be output by the 6500 when next addressed to talk. The program codes used to select output data are :

RA/B/R	READ BRIGHTLINE AMPLITUDE A/B/R
RF	READ BRIGHTLINE FREQUENCY
RS	READ STATUS
RX	READ EXTENDED STATUS
RMK	READ MARKER POSITIONS
RK	READ KEY CODE
RP	READ BRIGHTLINE POSITION
RDA/B/R	READ AMPLITUDE DISPLAY PARAMETERS A/B/R
RDF	READ FREQUENCY DISPLAY PARAMETERS
RMA/B/R	READ ASCII MEASUREMENT CHANNEL A/B/R
SHRMA/B/R	READ ASCII MEASUREMENT MEMORY A/B/R
RYA/B/R	READ BINARY MEASUREMENT CHANNEL A/B/R
SHRYA/B/R	READ BINARY MEASUREMENT MEMORY A/B/R
DPA/B	READ DIGITAL PLOT STRING TRACE A/B
DPG	READ DIGITAL PLOT STRING GRATICULE
DPL	READ DIGITAL PLOT STRING LABELS
RI	READ INSTRUMENT SETTINGS STORE

10. One of the above commands must be sent before addressing 6500 to talk. The format of the data output depends on the command sent. Some outputs may be read as numeric or string data, others may only be read as string data. In some cases the data is terminated with a CR LF sequence, in others it is terminated with the EOI signal. See individual command descriptions for more detailed information.

<u>Command description format</u>

11. For the purposes of detailed description the commands are divided into functional groups. In each case the detailed description consists of the following parts :

TITLE OF FUNCTIONAL GROUP
LIST OF COMMANDS DESCRIBED (with corresponding keys)
DEFINITION OF COMMAND SYNTAX (with examples)
GENERAL DESCRIPTION OF COMMAND(S)
REFERENCE TO RELATED SECTIONS (where appropriate)

The following conventions are used :

<..> Indicates a compulsory argument
[..] Indicates an optional argument or a front panel key legend

12. Application examples are given for HP Series 200 and, where appropriate, HP85 controllers in Chapter 4. The HP Series 200 range consists at present of 9816, 9826, 9836 and 9920 models and the examples given will run on any of these machines. The examples are given in the BASIC language and do not require any Series 200 BASIC extensions or HP85 enhancement ROMs other than the I/O ROM which is necessary for GPIB operation and the Advanced Programming ROM which allows the examples to be presented as sub-programs.

Measurement mode selection

13. *COMMANDS DESCRIBED* | *CORRESPONDING KEYS*

COMMANDS DESCRIBED	CORRESPONDING KEYS
CA CB CR CC	[A] [B] [R] [A&B]
SLR U	[-R] [UNITS]
SHCA SHCB SHCR	[MEM A] [MEM B] [MEM R]

COMMAND SYNTAX

These commands do not require any arguments.

COMMAND DESCRIPTION

These commands define the fundamental operating mode of the instrument and have the following individual functions :

CA	Select absolute power measurement on channel A
CB	Select absolute power measurement on channel B
CR	Select absolute power measurement on channel R
CC	Select absolute power measurement on channels A&B
SLR	Subtract live reference (-R)
U	Change measurement units - toggles between dBm/mW and dB/VSWR
SHCA	Display memory A
SHCB	Display memory B
SHCR	Display memory R

RELATED SECTIONS

MEMORY OPERATION (14)
READING STATUS INFORMATION (26)

Memory operation

14. *COMMANDS DESCRIBED* | *CORRESPONDING KEYS*

COMMANDS DESCRIBED	CORRESPONDING KEYS
STA STB STR STC	[STORE]
SHSTA SHSTB SHSTR SHSTC	[STORE AV]
SBA SBB SBR	[SUB MEM]

COMMAND SYNTAX

The normal key-stroke arguments corresponding to these commands are built into the commands themselves (i.e. STA is equivalent to the key sequence [STORE] [A]). These commands are the only exception to the general key-stroke compatibility policy.

COMMAND DESCRIPTION

STA	Store trace to memory A
STB	Store trace to memory B
STR	Store trace to memory R
STC	Store traces to memories A and B
SHSTA	Store average to memory A
SHSTB	Store average to memory B
SHSTR	Store average to memory R
SHSTC	Store averages to memories A and B
SBA	Subtract memory A
SBB	Subtract memory B
SBR	Subtract memory R

The validity of memory operations depends on the current measurement mode. Vol. 1 of the operating manual gives a table of valid memory operations. This table is reproduced below showing valid memory commands corresponding to each measurement mode.

CHANNEL	*A*	*B*	*A&B*	*R*
Valid store commands	[SH] STA [SH] STB [SH] STR	[SH] STA [SH] STB [SH] STR	[SH] STC	[SH] STA [SH] STB [SH] STR
Valid subtract commands	SBA SBR	SBB SBR	SBA SBB SBR	

The STORE AV and SUB MEM commands assume that valid data exists in the memory being accessed.

RELATED SECTIONS

MEASUREMENT MODE SELECTION (13)
READING STATUS INFORMATION (26)

Amplitude scaling

15. *COMMANDS DESCRIBED* / *CORRESPONDING KEYS*

SD SR	[DATUM] [RANGE]
AR	[AUTO]
SH8 SH9	[dB REL A] [dB REL B]

COMMAND SYNTAX	*EXAMPLE*
SD<DATUM VALUE>E	SD-12.5E
SR<RANGE VALUE>E	SR1.5E
AR requires no argument	
SH8 [dB REL A OFFSET] E	SH820E
SH9 [dB REL B OFFSET] E	SH9-35.5E

COMMAND DESCRIPTION

SD	Set Datum (Range: -99.9 to +99.9dB(m) Res: 0.1dB)
SR	Set Range (Range: +0.1 to +10.9dB(m) Res: 0.1dB)
AR	Auto Range (selects optimum DATUM and RANGE values)
SH8	Set dB REL A (Range: -99.9 to +99.9dB Res: 0.01dB)
SH9	Set dB REL B (Range: -99.9 to +99.9dB Res: 0.01dB)

The dB REL commands do not actually alter the amplitude scaling, but the specified offset is added to the measurement data. If no argument is supplied (e.g. SH8E) then the inverse of the current brightline reading is used. This allows the current brightline point to be used as a 0 dB reference without having to enter the required value.

RELATED SECTIONS

READING DISPLAY PARAMETERS (27)

Frequency scaling

16. *COMMANDS DESCRIBED* / *CORRESPONDING KEYS*

COMMANDS DESCRIBED	CORRESPONDING KEYS
SS SP	[START] [STOP]
SHSS SHSP	[F1] [F2]
FW	[F1-F2]
DF	[DELTA F]
SH-	[SECRET]

COMMAND SYNTAX	*EXAMPLE*
SS [START FREQUENCY] E	SS2.05E
SP [STOP FREQUENCY] E	SP12.45E
FW Requires no argument	
DF [SWEEP WIDTH] E	DF1.5E
SH- Requires no argument	

COMMAND DESCRIPTION

SS	Set Start Frequency (Range: F1 to STOP Res: 0.01GHz)
SP	Set Stop Frequency (Range: START to F2 Res: 0.01GHz)
SHSS	Set Sweeper F1 (Range: 0 to +126GHz Res: 0.01GHz)
SHSP	Set Sweeper F2 (Range: 0 to +126GHz Res: 0.01GHz)
FW	Set START and STOP to current F1 and F2 values
DF	Set symmetrical swbep about brightline frequency (Sweep Width Range: F2-F1 Res: 0.01GHz)
SH-	Toggle SECRET mode

F1, F2, START and STOP frequency values must always satisfy the following convention:

F1 <= START <= STOP <= F2

If no argument is specified for F1 or F2 no action is taken but the current setting is echoed on the CRT. If no argument is specified for START or STOP the current brightline frequency is used. When the FW command is sent the current START and STOP settings are lost if they are different to F1 and F2.

The SH- command toggles in and out of SECRET mode. In SECRET mode the frequency scaling information is removed from the CRT.

RELATED SECTIONS

READING DISPLAY PARAMETERS (27)

Sweep mode selection

17. *COMMANDS DESCRIBED* / *CORRESPONDING KEYS*

Command	Key
N	[NORMAL]
AV	[AVERAGE]
FZ	[FREEZE]
SHN	[SPEED]

COMMAND SYNTAX	*EXAMPLE*
N Requires no argument	
AV Requires no argument	
FZ Requires no argument	
SHN<SWEEP SPEED NUMBER>	SHN5

COMMAND DESCRIPTION

N Select NORMAL sweep operation
AV Select AVERAGE sweep mode
FZ Toggle FREEZE mode
SHN Select sweep speed (Range: 0 to 9 as SPEED menu)

The N command is a general command for returning to NORMAL sweep operation. In addition to its use as an exit from AVERAGE and FREEZE modes, NORMAL can be used to abort CALAID, PLOT and STATUS modes, and any prompted command. On receipt of the N command, the 6500 switches off AVERAGE or FREEZE mode if applicable, resets the CRT display and re-starts the sweep.

The AV command selects sweep averaging (see Vol. 1 for details). Averaging is re-started each time the command is sent.

The FZ command toggles between the current sweep mode and FREEZE mode. If the current sweep mode is AVERAGE the averaging process is not re-started on toggling out of FREEZE.

The argument for the SHN command is a single digit in the range 0 to 9 corresponding to the sweep speed menu numbers. These allow sweep speeds from 70 ms (0) to 20 s (9). The power-on value is 100 ms (1). Note that the 70 ms sweep mode incurs a 50% reduction in measurement resolution.

RELATED SECTIONS

READING STATUS INFORMATION (26)

Display mode selection

18. *COMMANDS DESCRIBED*	*CORRESPONDING KEYS*
H	[HIST]
L	[LINE]

COMMAND SYNTAX

These commands do not require any arguments.

COMMAND DESCRIPTION

H   Select HISTOGRAM display mode
L   Select LINE display mode

The H and L commands operate on the currently displayed channel(s). The display mode for any channel will only be affected when an H or L command is executed while that channel is displayed. The display modes for each channel are undefined at power on.

RELATED SECTIONS

MEASUREMENT MODE SELECTION (13)

Limit checking facilities

19. *COMMANDS DESCRIBED*	*CORRESPONDING KEYS*
SHSD SHSR	[HIGH] [LOW]
SH7	[LIMITS]

COMMAND SYNTAX	*EXAMPLE*
SHSD<HIGH LIMIT VALUE>E	SHSD3.72E
SHSR<LOW LIMIT VALUE>E	SHSR-30E
SH7 Requires no argument	

COMMAND DESCRIPTION

SHSD   Set High Limit (-99.99 to +99.99 dB(m) Res: 0.01dB)
SHSR   Set Low Limit (-99.99 to +99.99 dB(m) Res: 0.01dB)
SHS7   Enable/Disable limit checking

Although limit values are always entered in dB(m) limit checking may still be performed in mW or VSWR modes when the limit values will be assumed to be in mW or VSWR.

Limit checking is enabled and disabled with the SH7 command which has a toggle action. The 'enabled' condition is indicated by the letter 'L' displayed in the top left corner of the CRT, immediately above the amplitude units indicator.

Limit checking is performed only on the channel(s) currently displayed. When a limit is exceeded an appropriate warning message is displayed on the top line of the CRT. The 6500 may also be programmed to issue an SRQ on this condition.

RELATED SECTIONS

READING DISPLAY PARAMETERS (27)
READING STATUS INFORMATION (26)
SRQ FACILITIES (32)

X-Y Plotter control

20. *COMMANDS DESCRIBED* — *CORRESPONDING KEYS*

COMMANDS DESCRIBED	CORRESPONDING KEYS
P	[PLOT]

COMMAND SYNTAX

The P command requires no argument, but invokes a menu driven plot sequence which is described below.

COMMAND DESCRIPTION

Assuming the 6500 is not in 'TALK ONLY' mode (see DIGITAL PLOTTER CONTROL) the P command generates an analog plotter control menu as follows:

0 - Plot All
1 - Pen Bottom Left
2 - Pen Top Right
3 - Pen to Origin
4 - Draw Axes
5 - Label Axes
6 - Plot
7 - Set Pen Lift
8 - Set Plot Speed
9 - Set Live Y

Option 0 causes options 4, 5 and 6 to be performed in sequence, producing a plot with labelled axes. Options 1, 2 and 3 are used to set up the plotter input scaling. Option 7 is used to set the logical sense of the pen lift output. A secondary menu is generated with the following options :

1 - Normal
2 - Invert

Option 8 of the primary menu allows selection of the plot speed. This is useful when using plotters which suffer from 'overshoot' problems. A plot speed number from 1 to 9 must be entered. The currently selected speed is indicated.

Option 9 allows the user to set up the plotter Y output to drive a chart recorder. A secondary menu is generated :

1 - Off
2 - On

All option numbers are sent over the bus as single ASCII digits. As some of the procedures require some time for execution two methods of ascertaining when the 6500 is waiting for an option number entry are provided. One is an SRQ facility and the other is part of the extended status message.

RELATED SECTIONS

DIGITAL PLOTTER CONTROL (21)
READING STATUS INFORMATION (26)
SRQ FACILITIES (32)

Digital plotter control

21.	*COMMANDS DESCRIBED*	*CORRESPONDING KEYS*
	DPA DPB DPG DPL	-

COMMAND SYNTAX

These commands do not require any arguments.

COMMAND DESCRIPTION

DPA Read HPGL string for Trace A
DPB Read HPGL string for Trace B
DPG Read HPGL string for Graticule
DPL Read HPGL string for labels

The DPA, DPB, DPG and DPL commands allow the controller to read the HPGL strings associated with trace A, trace B, graticule and labels which would normally be sent directly to the plotter when in 'TALK ONLY' mode. On receipt of one of thee commands the 6500 will output the appropriate strings when next addressed to talk. The strings are terminated with CRLF and the EOI signal. The strings associated with traces are a fixed length of 3418 bytes. The graticule and label strings may vary in length from 350 to 1100 and 150 to 500 characters respectively depending on display content. The strings may be sent directly to a HPGL plotter or stored for later use. Appendix G gives scaling information to allow modifications to be made to the strings (e.g. to add a title).

Digital plot in TALK ONLY mode

The talk only facility allows a digital plotter to be driven by the 6500 in a "stand alone" configuration provided it is compatible with the following HPGL command subset.

DF Set default
SC Scale
SR Set relative character size
PA Plot absolute
PU Pen up
PD Pen down
LB Label
SP Select pen*

* Plotters with only one pen may be used although a plotter with two pens is preferable.

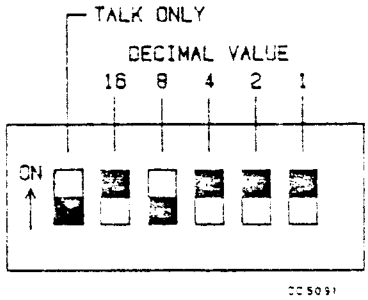
The digital plotter facilities are made available as follows:-

(1) Select the plotter to the Listen only mode (see Plotter manufacturer's Instruction Manual for details of this).

(2) Before switching 6500 power on, select the GPIB Address switch to Talk only mode.

Note...

When the 6500 is in the Talk only mode it must not be connected to a controller or to any other GPIB instrument other than a HPGL compatible plotter set to Listen only mode. This is important as a hardware bus conflict could arise. When connecting a 6500 to a controller driven system remember to check that the Talk only mode is not selected.



(3) Switch on 6500, press PLOT key which will present the following menu:

0 - Plot all
1 - Draw graticule *
2 - Label graticule **
3 - Plot
4 - Set live Y ***

* Draw graticule, a representation of the 6500 is plotted with the brightline and markers included and distinguishable from the vertical graticule lines.

** Label graticule. The following annotation is added around the graticule:

(i) Sweep speed.
(ii) Vertical scale units.
(iii) Vertical scaling.
(iv) Frequency scaling (except when SECRET mode is selected).
(v) Brightline spot measurements.
(vi) Measurement details.

Two pen colours are used to improve clarity on two channel plots.

*** Live Y. This menu option is duplicated from the analogue X Y plotter menu to allow 'Live Y output' to be selected. See Appendix H for sample of digital plot.

RELATED SECTIONS

X-Y PLOTTER CONTROL (20)
APPENDIX G and H

Instrument settings control

22. *COMMANDS DESCRIBED*	*CORRESPONDING KEYS*
SH5 SH6	[STO] [RCL]
RI WI	-

COMMAND SYNTAX	*EXAMPLE*
SH5<DESTINATION STORE>	SH53
SH6<SOURCE STORE>	SH61
RI<SOURCE STORE>	RI9
WI<DESTINATION STORE><BINARY DATA>	See APPLICATIONS (Chap. 4)

COMMAND DESCRIPTION

SH5 Store current instrument settings to specified store
SH6 Recall instrument settings from specified store
RI Instruct 6500 to send binary data from specified store
WI Write binary data to specified store

In all cases the source/destination store is a number in the range 1-9. SH5 causes the current instrument settings to the specified store. The following parameters are stored :

F1, F2, START, STOP
DATUM A, DATUM B, DATUM R, RANGE A, RANGE B, RANGE R
LIMIT CHECKING ON/OFF
HIGH LIMIT A, HIGH LIMIT B, LOW LIMIT A, LOW LIMIT B
dB REL A, dB REL B
SWEEP SPEED
AVERAGING ON/OFF
MARKER POSITIONS
MEASUREMENT MODE (Channels, Memory usage, Units, Etc.)
TEMPERATURE CORRECTION ON/OFF
DETECTOR TYPES

Once stored, these instrument settings can be recalled with SH6. The 6500 stores the settings internally as a binary data block. This can be read over the bus with the RI command. The data is sent as a 58 byte string conforming to the block data transfer format specified in IEEE 728-1982 as follows :

#JBBB....BBBC

Where : #J indicates a binary transfer format (IEEE 728-1982)
B is an 8 bit binary value
C is a checksum byte

The data can be sent back to any store with the WI command. The data is intended for storage/retrieval only and should not be altered. The 6500 will not accept a data transfer with an invalid checksum byte. Note that in both directions the transfer is terminated by asserting the EOI signal with the last byte.

Brightline positioning

23. *COMMANDS DESCRIBED* | *CORRESPONDING KEYS*

COMMANDS DESCRIBED	*CORRESPONDING KEYS*
BR BL	ROTARY CONTROL
BP	-
MX MN	[MAX] [MIN]
RP	-

COMMAND SYNTAX	*EXAMPLE*
BR Requires no argument	
BL Requires no argument	
BP<BRIGHTLINE POSITION>E	BP123E
MX Requires no argument	
MN Requires no argument	
RP Requires no argument	

COMMAND DESCRIPTION

BR	Move brightline one position right
BL	Move brightline one position left
BP	Move brightline to specified position (Range : 0 to 421)
MX	Move brightline to MAX point on displayed trace(s)
MN	Move brightline to MIN point on displayed trace(s)
RP	Instruct 6500 to output current brightline position

The trace display is divided into 422 brightline measurement positions and 211 physical brightline positions. Brightline control is implemented in terms of measurement position at all times. Thus multiple BL or BR commands will only move the brightline physically on alternate executions, but each execution will move the brightline to a new measurement position.

The RP command causes the 6500 to output the current brightline measurement position as a 3 digit number in the range 0 to 421 terminated with CRLF and EOI.

The 6500 can be programmed to issue an SRQ on manual operation of the brightline control when in the remote state.

RELATED SECTIONS

MARKER CONTROL (24)
BRIGHTLINE DATA TRANSFER (25)
SRQ FACILITIES (32)

Marker control

24. *COMMANDS DESCRIBED* — *CORRESPONDING KEYS*

Commands	Keys
MK SHMK	[MARKER] [ERASE]
RMK	-

COMMAND SYNTAX

These commands do not require any arguments.

COMMAND DESCRIPTION

MK Place marker at current brightline position
SHMK Erase all markers
RMK Read marker positions

A maximum of eight markers can be placed using the MK command. Markers are placed at the current brightline position and are displayed as vertical lines on the CRT similar in appearance to the brightline itself. Markers can be erased individually by placing the brightline over a displayed marker and executing MK. Alternatively, all markers can be erased with SHMK.

The RMK command causes the 6500 to output a 31 byte string consisting of eight three-digit numbers separated by commas as follows :

NNN,NNN,NNN,NNN,NNN,NNN,NNN,NNN

Each number represents the current display position of a marker in the range 0 to 210. A value of 999 indicates that the marker is not currently in use. The output string is terminated with CRLF and EOI.

RELATED SECTIONS

BRIGHTLINE POSITIONING (23)

Brightline data transfer

25. *COMMANDS DESCRIBED* — *CORRESPONDING KEYS*

Commands	Keys
RA RB RR RF	-
WD	-

COMMAND SYNTAX	*EXAMPLE*
RA Requires no argument	
RB Requires no argument	
RR Requires no argument	
RF Requires no argument	
WD<DATA VALUE>E	WD-30.5E

COMMAND DESCRIPTION

RA Read channel A amplitude at brightline position
RB Read channel B amplitude at brightline position
RR Read channel R amplitude at brightline position
RF Read frequency at brightline position
WD Write data to displayed channel at brightline position

RA, RB and RR cause the 6500 to output the current brightline amplitude of the A, B or R channels (which do not have to be currently displayed). The value is output in current units and has a fixed format :

SDD.DD

where S is a sign,
D is a digit 0 - 9.

RF causes the 6500 to output the current brightline frequency in GHz in the following fixed format :

SDDD.DD

The WD command allows amplitude data to be written to the currently displayed trace. The data should conform to NR2 format as defined in IEEE 728-1982 and must be terminated with 'E'. The display must be in FREEZE mode. Data is written to the current brightline position and is assumed to be in current units. When both A and B traces are displayed, the data is written to channel A only.

RELATED SECTIONS

BRIGHTLINE POSITIONING (23)
SWEEP MODE SELECTION (17)

Reading status information

26. *COMMANDS DESCRIBED* — *CORRESPONDING KEYS*

RS RX — -

COMMAND SYNTAX

These commands do not require any arguments.

COMMAND DESCRIPTION

RS causes the 6500 to output a 10 character string containing status information as follows :

NNNNNNNNNN

- Units : 0=dBm 1=mW 2=dB 3=VSWR M=Memory display
- Limit checking : 0=OFF 1=ON
- Freeze Mode : 0=OFF 1=ON
- Averaging Mode : 0=OFF 1=ON
- Sweep Speed.: 0-9 corresponding to menu number
- Valid Data flag : 0=Data invalid 1=Data valid
- Number of last error detected (00=none)
- Number of current error (00=none)

RX causes the output of a 24 character string consisting of the above plus 14 additional characters defined as follows :

NNNNNNNNNNNNNN

- 6500 Firmware Issue Number
- Detector type ABR. Each digit identifies the detector type by the last digit of its type number (i.e. 1=6511 4=6514 etc.).
- Temperature Correction : 0=OFF 1=ON
- Memory status : (may be combined to give 0-7)
  - 0 - All memories null
  - 1 - Memory A valid
  - 2 - Memory B valid
  - 4 - Memory R valid
- Live Y output : 0=OFF 1=ON
- Plot Speed : 1-9 as defined in plot menu
- Pen Lift Sense : 0=Normal 1=Inverted
- Plot mode : 0=Inactive 1=Awaiting Command 2=Busy
- Measurement Mode : (may be combined to give 00-63)
  - 00 - Absolute power
  - 01 - Sub Mem A
  - 02 - Sub Mem B
  - 04 - Sub Mem R
  - 08 - -REF
  - 16 - dB REL A
  - 32 - dB REL B
- Display Mode :
  - 0 - Channel A
  - 1 - Channel B
  - 2 - Channel R
  - 3 - Channels A&B
  - 4 - MEM A
  - 5 - MEM B
  - 6 - MEM R
  - 7 - CALAID

RELATED COMMANDS

The use of RS and RX is discussed in APPLICATIONS (Chap. 4).

Reading display parameters

27. *COMMANDS DESCRIBED* — *CORRESPONDING KEYS*

RDA RDB RDR RDF — -

COMMAND SYNTAX

These commands do not require any arguments.

COMMAND DESCRIPTION

Each of these commands causes the 6500 to output a string containing numeric values separated by commas. The values output are as follows :

RDA	DATUM A,	RANGE A,	HIGH LIM A,	LOW LIM A	(dB)
RDB	DATUM B,	RANGE B,	HIGH LIM B,	LOW LIM B	(dB)
RDR	DATUM R,	RANGE R,	dB REL A,	dB REL B	(dB)
RDF	F1 ,	F2 ,	F START ,	F STOP	(GHz)
RDM	Δ MARKER/BRIGHTLINE A,		Δ MARKER/BRIGHTLINE B		(dB)

For RDA, RDB and RDR a 27 byte string is output in the following format :

SDD.DD,SDD.DD,SDD.DD,SDD.DD

For RDF a 31 byte string is output as follows :

SDDD.DD,SDDD.DD,SDDD.DD,SDDD.DD

For RDM a string of the form

SDD.DD or SDD.DD,SDD.DD

is output, depending on whether one or both measurement channels are in use.

In each case S indicates a sign, D indicates a digit and the string is terminated with CRLF and EOI.

RELATED SECTIONS

AMPLITUDE SCALING (15)
FREQUENCY SCALEING (16)
LIMIT CHECKING FACILITIES (19)

ASCII measurement transfer

28. *COMMANDS DESCRIBED* *CORRESPONDING KEYS*

RMA RMB RMR SHRMA SHRMB SHRMR	-
WMA WMB WMR SHWMA SHWMB SHWMR	-

COMMAND SYNTAX

ASCII read commands (prefix R or SHR) require no parameters . ASCII write commands (prefix W or SHW) must be followed by a block of ASCII values as described below.

COMMAND DESCRIPTION

RMA	Read ASCII measurement from channel A
RMB	Read ASCII measurement from channel B
RMR	Read ASCII measurement from channel R
SHRMA	Read ASCII measurement from memory A
SHRMB	Read ASCII measurement from memory B
SHRMR	Read ASCII measurement from memory R

In each case the data output consists of 422 values separated by commas forming a 2953 byte string as follows :

SDD.DD,SDD.DD, ... ,SDD.DD,SDD.DD
1st value, ... ,422nd value

Where S indicates a sign and D indicates a digit. The string is terminated with CRLF and EOI.

WMA	Write ASCII measurement to channel A
WMB	Write ASCII measurement to channel B
WMR	Write ASCII measurement to channel R
SHWMA	Write ASCII measurement to memory A
SHWMB	Write ASCII measurement to memory B
SHWMR	Write ASCII measurement to memory R

In each case the command must be followed by 422 data values conforming to NR2 or NR3 formats as defined in IEEE 728-1982 separated by commas and terminated with CRLF, LF only or EOI.

Note that measurements may be transferred to any channel or memory irrespective of whether it is currently being displayed. When writing to a channel the 6500 should be in FREEZE mode in order to retain the data.

RELATED SECTIONS

BINARY MEASUREMENT TRANSFER (29)
ASCII transfers are discussed in APPLICATIONS (Chap. 4).

Binary measurement transfer

29. *COMMANDS DESCRIBED* | *CORRESPONDING KEYS*

Commands	Keys
RYA RYB RYR SHRYA SHRYB SHRYR	-
WYA WYB WYR SHWYA SHWYB SHWYR	-

COMMAND SYNTAX

Binary read commands (prefix R or SHR) require no parameters. Binary write commands (prefix W or SHW) must be followed by a binary data block as described below.

COMMAND DESCRIPTION

RYA	Read binary measurement from channel A
RYB	Read binary measurement from channel B
RYR	Read binary measurement from channel R
SHRYA	Read binary measurement from memory A
SHRYB	Read binary measurement from memory B
SHRYR	Read binary measurement from memory R

In each case the data output consists of an 846 byte string formatted as follows :

#IBBBB .... BBBB

Where #I indicates a binary transfer format which is defined in IEEE 728-1982. B is an 8 bit binary byte. There are 422 pairs of bytes which contain data values conforming to the 6500 internal 16 bit data format. The string is terminated by asserting the EOI signal with the last data byte.

WYA	Write binary measurement to channel A
WYB	Write binary measurement to channel B
WYR	Write binary measurement to channel R
SHWYA	Write binary measurement to memory A
SHWYB	Write binary measurement to memory B
SHWYR	Write binary measurement to memory R

In each case the command must be followed by a binary data block as described above. The 6500 will only terminate binary data input with the EOI signal which should be asserted with the last data byte. The binary transfer facility is intended for applications where no manipulation of the data is required, although a technique for extracting the measurement values is described in APPLICATIONS (Chap. 4). The main advantage of binary over ASCII transfers is an approximate 5:1 speed improvement. (The actual transfer times depend on the GPIB controller being used - see Chap. 4).

RELATED SECTIONS

ASCII MEASUREMENT TRANSFER (28)
Binary transfers are discussed in APPLICATIONS (Chap. 4).

Text display control

30. *COMMANDS DESCRIBED* | *CORRESPONDING KEYS*

WT TX DA | -

COMMAND SYNTAX | *EXAMPLE*

WT<TEXT>$ | WTBand Pass Filter$
TX<"TEXT"> | TX"Press [ENTER] :"
· DA Requires no argument

COMMAND DESCRIPTION

WT is used to write a title to the top line of the CRT (overwriting the measurement mode indicator) with a maximum length of 28 characters. All printable ASCII characters may be used except '$' which is used as a terminator.

TX may be used to write text anywhere on the 6500 CRT. The 6500 maintains a 'text pointer' similar to a cursor on a VDU. Text written with TX will always start at the current text pointer position. The position of the text pointer is incremented by one column (horizontally) with each character of the text until the end of the current row (column 40) is reached. All subsequent text will overwrite the last character on the row. The text pointer may be manipulated in various ways with ASCII codes 0 to 15 which are reserved as control codes. A full list of these is given in Appendix C. Control facilities include :

Text pointer move in any direction
Clear screen/row
Set/Reset tab stops
Enable/Disable flashing characters

All standard ASCII characters plus 16 special characters are available. A table showing these is given in Appendix C. There is no limit to the length of the text but in order to comply with the text transfer format defined in IEEE 728-1982 it must be contained within quotes (").

The DA command switches off all display elements except alphanumerics. Thus text can be written over existing annotation or the CRT can be used simply as a VDU. Appendix E contains a blank CRT layout chart (the CRT format is 24 rows of 40 columns) and Appendix F contains layout charts showing the positions of normal 6500 annotation and messages. Normal display mode may be resumed with the N (NORMAL) command.

RELATED SECTIONS

APPENDICES C,E,F
Text control is discussed in APPLICATIONS (Chap. 4).

Keyboard control

31. *COMMANDS DESCRIBED* *CORRESPONDING KEYS*

COMMANDS DESCRIBED	CORRESPONDING KEYS
RK XK	-

COMMAND SYNTAX

These commands do not require any arguments.

COMMAND DESCRIPTION

RK Read last key pressed
XK Execute last key read by RK

The RK command is normally used in conjunction with the 'SRQ on key press' facility (see SRQ FACILITIES) to intercept key presses while the 6500 is under remote control. The 6500 will output a number in the range 0 to 38 indicating which key was pressed. In order to make the interpretation of numeric data entry easier the numeric keys 0 to 9 are assigned key codes 0 to 9. APPENDIX D shows the keyboard layout indicating all the key codes.

When a key code has been read with RK the XK command may be used to make the 6500 execute the procedure associated with that key as though it had been pressed under local control. Using this technique it is possible to inhibit certain keys, or add extra user-prompts and facilities to an instrument apparently operating under local control. These ideas are discussed further in APPLICATIONS (Chap. 4).

RELATED SECTIONS

SRQ FACILITIES (32)
APPENDIX D

SRQ facilities

32. *COMMANDS DESCRIBED* — *CORRESPONDING KEYS*

COMMANDS DESCRIBED	*CORRESPONDING KEYS*
SQ	-

COMMAND SYNTAX	*EXAMPLE*
SQ<SRQ MASK>	SQ10000

COMMAND DESCRIPTION

The SRQ mask allows SRQ interrupts to be enabled/disabled for any combination of five events. The mask consists of a 5 digit ASCII string. Each digit should be either 0 to disable the function or 1 to enable it. The functions are arranged as follows :

```
NNNNN
|||||
||||└──── SRQ on plot menu option requirement
|||└───── SRQ on front panel operation
||└────── SRQ on limits exceeded
|└─────── SRQ on error condition
└──────── SRQ on end of sweep
```

When one of the enabled conditions occurs, an SRQ will be issued. The controller should respond with a SERIAL POLL interrogation. The 6500 will then output a STATUS BYTE. The STATUS BYTE is interpreted as follows :

```
Bit : 76543210
      ||| └──── Decimal value indicates SRQ event (see below)
      ||└────── Not used (always 0)
      |└─────── 2 indicates SRQ issued by 6500
      └──────── Not used (always 0)
```

The decimal value of bits 0-3 is interpreted as follows :

0	Not used
1	Key press
2	Brightline control rotated left
3	Brightline control rotated right
4-9	Not used
10	End of sweep
11	Limits exceeded (only if limits enabled)
12	Error condition
13	Plot menu option requirement
14-15	Not used

Note...

PARALLEL POLL is not supported in 6500.

RELATED SECTIONS

The use of SRQ facilities is discussed further in APPLICATIONS (Chap. 4).

Synthesizer mode

33. *COMMANDS DESCRIBED*	*CORRESPONDING KEYS*
SH2 SH3	-

COMMAND SYNTAX

These commands do not require any arguments.

COMMAND DESCRIPTION.

The Synthesizer Mode commands are provided to allow the use of GPIB programmable frequency synthesizers where no external ramp input facility exists. Synthesizer mode is entered with the SH2 command. The 6500 now operates as normal except that it waits for the SH3 command before making a new measurement. Thus 422 SH3 commands are required to perform a complete sweep. The controller must send appropriate frequency commands to the synthesizer in between each SH3 command execution. All normal measurement modes may be used. Note that some commands (SD, SR, SS, SP, AR, etc.) cause the 6500 to re-start its sweep. The controlling software must take account of this in order to maintain correct frequency tracking between the 6500 and the synthesizer. To exit from synthesizer mode use the N command.

RELATED SECTIONS

An example of Synthesizer Mode operation is given in APPLICATIONS (Chap. 4).

Miscellaneous functions

34. *COMMANDS DESCRIBED*	*CORRESPONDING KEYS*
SHAR	[ZERO]
SHFW	[DET]
SH1	[CALAID]
SH4	[STATUS]

COMMAND SYNTAX	*EXAMPLE*
SHAR Requires no argument	
SHFW<DETECTOR TYPES>E	SHFW114E
SH1 Requires no argument	
SH4 Requires no argument	

COMMAND DESCRIPTION

SHAR performs an AUTO-ZERO operation on the detectors. No r.f. power should be connected during this operation. An AUTO-ZERO operation MUST be performed after power on before any measurements are made. Consult Vol. 1 of the Operating Manual for further details.

SHFW is used to select appropriate error correction for the detector types being used. The argument is a 3 digit number where each number identifies the detector type by the last digit of its type number (i.e. 1=6511 4=6514 etc.). The 3 digits identify detector types for channels A, B and R respectively.

SH1 and SH4 are included for the sake of completeness but are not intended for remote operation. SH1 invokes the calibration aid facility (which can be aborted with the N command), and SH4 calls up the instrument status display. Both of these facilities are essentially manual functions and the user should consult Vol. 1 of the Operating Manual for further details of their operation.

RELATED SECTIONS

READING STATUS INFORMATION (26)

Chapter 4

APPLICATIONS

CONTENTS

INTRODUCTION

1. This chapter presents a set of example GPIB program routines which are designed to cover some of the common system requirements and to illustrate some of the advanced features of the 6500 GPIB facility. All the examples are presented as sub-programs or functions which may be incorporated directly into the user's programs. For each example an implementation is given for the HP Series 200 controller and, where appropriate, the HP85. All examples are fully commented. The comments (preceded by '!') may, of course, be omitted.

HP SERIES 200 IMPLEMENTATION

2. Currently the Series 200 range of controllers includes the following models:

9816 (216, Model 16)
9826 (226, Model 26)
9836 (236, Model 36)
9920 (220, Model 20)

The example routines will run on any of the above models with BASIC 2.0 installed. No language extensions are required. The example routines are presented as SUB-PROGRAMS or FUNCTIONS which provide a self-contained program context. The routines should be called with parameters where necessary. Parameters must be of the correct type (REAL, INTEGER or STRING). The main program should contain COM statements to match those in the sub-program and should perform variable initialization, I/O path assignments and array/string dimensioning as necessary. GPIB device addresses and status string variables are passed in COM statements. The following conventions have been adopted:

COM /A/ @Analyser	6500 GPIB address
COM /B/ Status$	6500 status string (24 chars.)
COM /C/ @Synthesizer	Synthesizer GPIB address
COM /D/ @Plotter	Plotter GPIB address

Consult the controller manuals for detailed information on programming semantics.

HP85 IMPLEMENTATION

3. The HP85 routines are presented as SUB-PROGRAMS, which require the ADVANCED PROGRAMMING ROM to be installed. This approach was adopted as it allows the routines to be presented in a convenient manner. For use without the AP ROM all the routines may be easily converted to normal BASIC sub-routines with the following procedure :

(a) Remove the SUB definition statement.

(b) Remove COM statements or replace with DIM statements if necessary.

(c) Replace SUBEXIT and, where appropriate, SUBEND statements with RETURN.

(d) Replace CALL statements with GOSUB statements to the appropriate line number for the routine being called.

Note that variables which are local to the sub-program will become global when the above procedure is followed.

4. In addition to the AP ROM the following hardware items are required for correct operation :

ROM DRAWER
I/O ROM
HPIB INTERFACE

For use as sub-programs the routines should be called with parameters where necessary and any COM statements in the sub-program should have matching COM statements in the main program. All variable initialization should be performed in the main program. GPIB addresses and status string variables are passed in COM statements. The following conventions have been adopted :

```
COM A1         6500 GPIB address
COM S$ [24]    6500 status string
COM A2         Synthesizer GPIB address
COM A3         Plotter GPIB address
```

Consult the controller manuals for full details of programming semantics.

DESCRIPTION FORMAT OF EXAMPLES

5. In addition to full listings of each implementation a description of each example is given using the following format :

Title and general description
Input requirements (formal parameters)
Output definitions (formal parameters)
Sub-program calls
Special considerations

Example 1 Valdat

6. This routine monitors 6500 status until the valid data flag is true. Measurement data becomes invalid under certain conditions (during AUTO RANGE, AUTO ZERO, etc.) and certain operations require data to be valid before they can be performed successfully. GPIB commands requiring valid data are :

[SH] STA [SH] STB [SH] STC FZ P MX MN

It is good practice to call Valdat before executing any of these commands.

Input requirements : NONE

Output definitions : NONE

Sub-program calls : NONE

HP85 Sub-program

```
1000 SUB "Valdat"
1010 COM A1
1020 COM S$[24]
1030 OUTPUT A1 ;"RS" !                                Tell 6500 to output status
1040 ENTER A1 ; S$ !                                  Read status string
1050 IF S$[5,5]<>"1" THEN WAIT 100 @ GOTO 1030 !      Repeat if data not valid
1060 SUBEND
```

HP200 Sub-program

```
10000 SUB Valdat
10010   COM /A/ @Analyser
10020   COM /B/ Status$
10030   LOOP                                 ! Checking loop
10040     OUTPUT @Analyser;"RS"              ! Tell 6500 to output status
10050     ENTER @Analyser;Status$            ! Read status string
10060   EXIT IF Status$[5,5]="1"             ! Exit loop if data valid
10070     WAIT .1                            ! Else wait 100mS
10080   END LOOP                             ! and try again
10090 SUBEND
```

Example 2   Freeze

7. This routine places 6500 into freeze mode. No action is taken if freeze mode is already active.

Input requirements : NONE

Output definitions : NONE

Sub-program calls : Valdat

HP85 Sub-program

```
1000 SUB "Freeze"
1010 COM A1
1020 COM S$[24]
1030 OUTPUT A1 ;"RS" !                          Tell 6500 to output status
1040 ENTER A1 ; S$ !                            Read status string
1050 IF S$[8,8]="1" THEN SUBEXIT !              Return if already in FREEZE mode
1060 CALL "Valdat" !                            Wait for valid data
1070 OUTPUT A1 ;"FZ" !                          Place in FREEZE mode
1080 SUBEND
```

HP200 Sub-program

```
10000 SUB Freeze
10010   COM /A/ @Analyser
10020   COM /B/ Status$
10030   OUTPUT @Analyser;"RS"                   ! Tell 6500 to output status
10040   ENTER @Analyser;Status$                 ! Read status string
10050   IF Status$[8,8]="1" THEN SUBEXIT        ! Return if already in FREEZE mode
10060   CALL Valdat                             ! Wait for valid data
10070   OUTPUT @Analyser;"FZ"                   ! Place in FREEZE mode
10080 SUBEND
```

Example 3 Autoz

8. This routine performs an AUTO ZERO operation and returns with a flag indicating success or failure.

Input requirements : NONE

Output definitions :	Series 200	HP85
Error flag (1 = failure)	see below	E

Sub-program calls : Valdat

The Series 200 version of this routine is implemented as a function and should be called by :

Variable=FNAutoz

HP85 Sub-program

```
1000 SUB "Autoz" (E)
1010 COM A1
1020 COM S$[24]
1030 OUTPUT A1 ;"N" !                       NORMAL clears any current errors
1040 CALL "Valdat" !                        Wait for valid data
1050 OUTPUT A1 ;"SHAR" !                    Initiate AUTO ZERO
1060 CALL "Valdat" !                        Wait for valid data
1070 IF S$[1,2]="42" THEN E=1 ELSE E=0 !    Set or clear error flag
1080 SUBEND
```

HP200 Sub-program

```
10000 DEF FNAutoz
10010   COM /A/ @Analyser
10020   COM /B/ Status$
10030   OUTPUT @Analyser;"N"               ! NORMAL clears any current error
10040   CALL Valdat                        ! Wait for valid data
10050   OUTPUT @Analyser;"SHAR"            ! Initiate AUTO ZERO
10060   CALL Valdat                        ! Wait for valid data
10070   IF Status$[1,2]="42" THEN          ! Check for failure
10080     Fail=1                           ! Set fail flag
10090   ELSE
10100     Fail=0                           ! or clear it
10110   END IF
10120   RETURN Fail
10130 FNEND
```

Example 4 Synth

9. This routine generates an autoranged sweep using the 6500 GPIB 'synthesizer' mode.

Input requirements :	Series 200	HP85
Start frequency	Fstart	F1
Stop frequency	Fstop	F2

Output definitions : NONE

Sub-program calls : NONE

Note that the AUTO RANGE function requires two sweeps, the first of which is not displayed.

In the example the synthesizer is assumed to accept frequency data in units of 10 kHz (e.g. Marconi 6812). The units conversion statement may need to be altered to suit other synthesizers.

HP85 Sub-program

```
1000 SUB "Synth" (F1,F2)
1010 COM A1
1020 COM A2
1030 OUTPUT A1 ;"SS";F1;"E" !               Set start frequency
1040 OUTPUT A1 ;"SP";F2;"E" !               Set stop frequency
1050 OUTPUT A1 ;"SH2" !                     Initiate synthesizer mode
1060 OUTPUT A1 ;"AR" !                      Initiate AUTO RANGE
1070 FOR S=1 TO 2 !                         Two sweeps required for AUTO
1080 WAIT 100 !                             Allow set up
1090 FOR P=0 TO 421 !                       Sweep loop
1100 F=F1+P*(F2-F1)/421 !                   Calculate frequency
1110 F=INT(F*100000+.5) !                   Convert to 10kHz units
1120 OUTPUT A2 ;F !                         Output to synthesizer
1130 WAIT 10 !                              Allow synthesizer to lock
1140 OUTPUT A1 ;"SH3" !                     Step 6500
1150 NEXT P !                               End of sweep loop
1160 NEXT S
1170 WAIT 100 !                             Allow processing
1180 OUTPUT A1 ;"FZ" !                      Freeze display
1190 SUBEND
```

HP200 Sub-program

```
10000 SUB Synth(Fstart,Fstop)
10010   COM /A/ @Analyser
10020   COM /C/ @Synthesizer
10030   OUTPUT @Analyser;"SS";Fstart;"E"                     ! Set start frequency (for display only)
10040   OUTPUT @Analyser;"SP";Fstop;"E"                      ! Set stop  frequency (for display only)
10050   OUTPUT @Analyser;"SH2"                               ! Initiate synthesizer mode
10060   OUTPUT @Analyser;"AR"                                ! Initiate AUTO RANGE
10070   FOR Sweep=1 TO 2                                     ! Two sweeps required for AUTO RANGE
10080     WAIT .1                                            ! Allow set up
10090     FOR Point=0 TO 421                                 ! Sweep loop
10100       Frequency=Fstart+Point*(Fstop-Fstart)/421        ! Calculate frequency
10110       Frequency=INT(Frequency*100000+.5)               ! Convert to 10kHz units
10120       OUTPUT @Synthesizer;Frequency                    ! Output to synthesizer
10130       WAIT .01                                         ! Allow synthesizer to lock
10140       OUTPUT @Analyser;"SH3"                           ! Step 6500
10150     NEXT Point                                         ! End of sweep loop
10160   NEXT Sweep
10170   WAIT .1                                              ! Allow processing
10180   OUTPUT @Analyser;"FZ"                                ! Freeze display
10190 SUBEND
```

Example 5 Maxmin

10. This routine returns the amplitude and frequency values of the brightline MAX and MIN functions. Markers are placed at the MAX and MIN positions.

Input requirements : NONE

Output definitions :	Series 200	HP85
MAX amplitude	Amax	V1
MAX frequency	Fmax	F1
MIN amplitude	Amin	V2
MIN frequency	Fmin	F2

Sub-program calls : Valdat

HP85 Sub-program

```
1000 SUB "Maxmin" (V1,F1,V2,F2)
1010 COM A1
1020 COM S$[24]
1030 CALL "Valdat" !                    Wait for valid data
1040 OUTPUT A1 ;"SHMK" !                Erase existing markers
1050 OUTPUT A1 ;"MX MK" !               Find MAX and place marker
1060 OUTPUT A1 ;"RA" !                  Read amplitude
1070 ENTER A1 ; V1
1080 OUTPUT A1 ;"RF" !                  Read frequency
1090 ENTER A1 ; F1
1100 OUTPUT A1 ;"MN MK" !               Find MIN and place marker
1110 OUTPUT A1 ;"RA" !                  Read amplitude
1120 ENTER A1 ; V2
1130 OUTPUT A1 ;"RF" !                  Read frequency
1140 ENTER A1 ; F2
1150 SUBEND
```

HP 200 Sub-program

```
10000 SUB Maxmin(Amax,Fmax,Amin,Fmin)
10010   COM /A/ @Analyser
10020   COM /B/ Status$
10030   CALL Valdat                     ! Wait for valid data
10040   OUTPUT @Analyser;"SHMK"         ! Erase existing markers
10050   OUTPUT @Analyser;"MX MK"        ! Find MAX and place marker
10060   OUTPUT @Analyser;"RA"           ! Read amplitude
10070   ENTER @Analyser;Amax
10080   OUTPUT @Analyser;"RF"           ! Read frequency
10090   ENTER @Analyser;Fmax
10100   OUTPUT @Analyser;"MN MK"        ! Find MIN and place marker
10110   OUTPUT @Analyser;"RA"           ! Read amplitude
10120   ENTER @Analyser;Amin
10130   OUTPUT @Analyser;"RF"           ! Read frequency
10140   ENTER @Analyser;Fmin
10150 SUBEND
```

Example 6 Blpos

11. This routine positions the brightline at a target frequency. If the target frequency is outside the current START/STOP frequency range no action is taken and the error flag is returned true.

Input requirements :	Series 200	HP85
Target frequency	Target	F
Output definitions :	Series 200	HP85
Error flag	Err_flag	E

Sub-program calls : NONE

HP85 Sub-program

```
1000 SUB "Blpos" (F,E)
1010 COM A1
1020 OUTPUT A1 ;"RDF" !                     Read start/stop frequencies
1030 ENTER A1 ; D,D,F1,F2
1040 IF F<F1 OR F>F2 THEN E=1 @ SUBEXIT !   If invalid F return with error
1050 E=0 !                                  Reset error flag
1060 P=INT((F-F1)/(F2-F1)*421+.5) !         Calculate brightline position
1070 OUTPUT A1 ;"BP";P;"E" !                Place brightline
1080 SUBEND
```

HP200 Sub-program

```
10000 SUB Blpos(Target,Err_flag)
10010   COM /A/ @Analyser
10020   OUTPUT @Analyser;"RDF"                          ! Read start/stop frequencies
10030   ENTER @Analyser;Dummy,Dummy,Fstart,Fstop
10040   IF Target<Fstart OR Target>Fstop THEN           ! Check target within limits
10050     Err_flag=1                                    ! Return with flag set if error
10060     SUBEXIT
10070   ELSE
10080     Err_flag=0                                    ! Reset error flag
10090   END IF
10100   Point=INT((Target-Fstart)/(Fstop-Fstart)*421+.5)  ! Calculate brightline position
10110   OUTPUT @Analyser;"BP";Point;"E"                 ! Place brightline
10120 SUBEND
```

Example 7 Mfreq

12. This routine returns the frequency values for each of the eight markers. Values for non-displayed markers are set to -1.

Input requirements : NONE

Output definitions :	Series 200	HP85
Marker frequency array	Frequency (*)	F( )

Sub-program calls : NONE

The frequency array should be dimensioned with 8 elements (0-7).

HP85 Sub-program

```
1000 SUB "Mfreq" (F())
1010 COM A1
1020 DIM P(7) !                                        Array for positions
1030 OUTPUT A1 ;"RDF" !                                Read start/stop frequencies
1040 ENTER A1 ; D,D,F1,F2
1050 S=F2-F1 !                                         Calculate frequency span
1060 OUTPUT A1 ;"RMK" !                                Read marker positions
1070 ENTER A1 ; P(0),P(1),P(2),P(3),P(4),P(5),P(6),P(7)
1080 FOR M=0 TO 7 !                                    For each marker
1090 IF P(M)=999 THEN F(M)=-1 ELSE F(M)=P(M)/210*S+F1 !   Calculate frequency (-1=unused)
1100 NEXT M
1110 SUBEND
```

HP200 Sub-program

```
10000 SUB Mfreq(Frequency(*))
10010   COM /A/ @Analyser
10020   ALLOCATE INTEGER Pos(7)                          ! Allocate array for positions
10030   OUTPUT @Analyser;"RDF"                           ! Read start/stop frequencies
10040   ENTER @Analyser;Dummy,Dummy;Fstart,Fstop
10050   Span=Fstop-Fstart                                ! Calculate frequency span
10060   OUTPUT @Analyser;"RMK"                           ! Read marker positions
10070   ENTER @Analyser;Pos(*)
10080   FOR Marker=0 TO 7                                ! For each marker
10090     IF Pos(Marker)=999 THEN                        ! Ignore if unused
10100       Frequency(Marker)=-1
10110     ELSE
10120       Frequency(Marker)=(Pos(Marker)/210)*Span+Fstart   ! Calculate frequency
10130     END IF
10140   NEXT Marker
10150   DEALLOCATE Pos(*)                                ! Discard position array
10160 SUBEND
```

Example 8 Dplot

13. This routine causes the current measurement display to be plotted on an HPGL compatible plotter.

Input requirements : NONE

Output definitions : NONE

Sub-program calls : Valdat

Note that the HPGL strings are transferred directly from the 6500 to the plotter. This eliminates the need for large string variable allocation in the controller. If it was required to modify the HPGL strings in any way then they would have to be read into the controller.

HP85 Sub-program

```
1000 SUB "Dplot"
1010 COM A1
1020 COM S$[24]
1030 COM A3
1040 A=A1-700 !                                              Find 6500 base address
1050 P=A3-700 !                                              Find plotter base address
1060 CALL "Valdat" !                                         Wait for valid data
1070 OUTPUT A1 ;"RX" !                                       Read extended status
1080 ENTER A1 ; S$
1090 M=VAL(S$[11,11]) !                                      Extract display mode value
1100 C$="DPG" !                                              Plot graticule
1110 GOSUB 2000
1120 C$="DPL" !                                              Plot labels
1130 GOSUB 2000
1140 IF M<>1 AND M<>5 THEN C$="DPA" @ GOSUB 2000 !           Plot trace A if required
1150 IF M=1 OR M=3 OR M=5 THEN C$="DPB" @ GOSUB 2000 !       Plot trace B if required
1160 SUBEXIT
2000 ! ----------------------------------------------------- Routine to transfer HPGL
2010 OUTPUT A1 ;C$ !                                         Send read command to 6500
2020 SEND 7 ; UNL TALK A LISTEN P !                          Set up direct transfer
2030 RESUME 7 !                                              Initiate transfer
2040 STATUS 7,2 ; S !                                        Wait for EOI
2050 IF NOT BIT(S,3) THEN 2040
2060 ABORTIO 7 !                                             Terminate transfer
2070 RETURN
2080 SUBEND
```

HP200 Sub-program

```
10000 SUB Dplot
10010   COM /A/ @Analyser
10020   COM /B/ Status$
10030   COM /D/ @Plotter
10040   STATUS @Analyser,3;Ana                                  ! Find 6500 base address
10050   Ana=Ana-700
10060   STATUS @Plotter,3;Pltr                                  ! Find plotter base address
10070   Pltr=Pltr-700
10080   CALL Valdat                                             ! Wait for valid data
10090   OUTPUT @Analyser;"RX"                                   ! Read extended status
10100   ENTER @Analyser;Status$
10110   Mode=VAL(Status$[11,11])                                ! Extract display mode value
10120   Command$="DPG"                                          ! Plot graticule
10130   GOSUB Xfer
10140   Command$="DPL"                                          ! Plot labels
10150   GOSUB Xfer
10160   IF Mode<>1 AND Mode<>5 THEN                             ! Plot trace A if displayed
10170     Command$="DPA"
10180     GOSUB Xfer
10190   END IF
10200   IF Mode=1 OR Mode=3 OR Mode=5 THEN                      ! Plot trace B if displayed
10210     Command$="DPB"
10220     GOSUB Xfer
10230   END IF
10240   SUBEXIT
10250 !--------------------------------------------------------!
10260 Xfer:                                                     ! Routine to transfer HPGL
10270 !--------------------------------------------------------!
10280   OUTPUT @Analyser;Command$                               ! Send read command to 6500
10290   SEND 7;UNL TALK Ana LISTEN Pltr DATA                    ! Initiate direct transfer
10300   REPEAT                                                  ! Wait for EOI
10310     Monitor=READIO(7,23)
10320   UNTIL BIT(Monitor,3)
10330   ABORT 7                                                 ! Terminate transfer
10340   RETURN
10350 SUBEND
```

Example 9 Readi

14. This routine reads a binary string representing the instrument settings from one of the nine settings stores.

Input requirements :	Series 200	HP85
Source settings store (1-9)	Sto	S

Output definitions :	Series 200	HP85
Binary instrument settings string	Set$	I$
Error flag	Err_flag	E

Sub-program calls: Valdat

The binary string is intended for storage/retrieval purposes only. The error flag is set if the source store number is outside the range 1-9 or if the store specified contained null data. Note the use of the EOI terminator with binary data.

HP85 Sub-program

```
1000 SUB "Readi" (S,I$,E)
1010 COM A1
1020 COM S$[24]
1030 IF S<1 OR S>9 THEN E=1 @ SUBEXIT !          Check validity of store number
1040 OUTPUT A1 ;"N" !                             Clear any current error
1050 CALL "Valdat"
1060 OUTPUT A1 ;"RI"&VAL$(S) !                    Send RI command to 6500
1070 ENTER A1 USING "#%,#%K" ; I$ !               Read settings string
1080 OUTPUT A1 ;"RS" !                            Check for null store error
1090 ENTER A1 ; S$
1100 IF S$[1,2]="56" THEN E=1 ELSE E=0 !          Set or clear error flag
1110 SUBEND
```

HP200 Sub-program

```
10000 SUB Readi(INTEGER Sto,Set$,Err_flag)
10010   COM /A/ @Analyser
10020   COM /B/ Status$
10030   IF Sto<1 OR Sto>9 THEN                    ! Check validity of store number
10040     Err_flag=1
10050     SUBEXIT
10060   END IF
10070   OUTPUT @Analyser;"N"                      ! Clear any current error
10080   CALL Valdat
10090   OUTPUT @Analyser;"RI"&VAL$(Sto)           ! Send RI command to 6500
10100   ENTER @Analyser USING "%,-K";Set$         ! Read settings string
10110   OUTPUT @Analyser;"RS"                     ! Read status
10120   ENTER @Analyser;Status$
10130   IF Status$[1,2]="56" THEN                 ! Check for null store error
10140     Err_flag=1                              ! Set error flag
10150   ELSE
10160     Err_flag=0                              ! or clear it
10170   END IF
10180 SUBEND
```

Example 10 Writei

15. This routine sends a binary string (normally obtained using the Readi routine) to one of the nine instrument settings stores.

Input requirements :	Series 200	HP85
Destination settings store	Sto	S
Binary settings string	Set$	I$

Output definitions :	Series 200	HP85
Error flag	Err_flag	E

Sub-program calls : Valdat

The error flag is set if the specified store is outside the range 1-9 or if any error occurs during data transfer (e.g. checksum error). Note the use of the EOI terminator with binary data.

HP85 Sub-program

```
1000 SUB "Writei" (S,I$,E)
1010 COM A1
1020 COM S$[24]
1030 IF S<1 OR S>9 THEN E=1 @ SUBEXIT !                  Check validity of store number
1040 OUTPUT A1 ;"N" !                                     Clear any current error
1050 CALL "Valdat"
1060 CONTROL 7,16 ; 129,NUM(I$[58,58]) !                  Set up EOL for EOI on last byte
1070 OUTPUT A1 USING "K" ; "WI"&VAL$(S)&I$[1,57] !        Send settings string
1080 CONTROL 7,16 ; 2,13,10 !                             Restore EOL setting
1090 OUTPUT A1 !                                          Ensure termination if error
1100 OUTPUT A1 ;"RS" !                                    Check for error condition
1110 ENTER A1 ; S$
1120 IF S$[1,2]<>"00" THEN E=1 ELSE E=0 !                 Set or clear error flag
1130 SUBEND
```

HP200 Sub-program

```
10000 SUB Writei(INTEGER Sto,Set$,Err_flag)
10010   COM /A/ @Analyser
10020   COM /B/ Status$
10030   IF Sto<1 OR Sto>9 THEN                               ! Check validity of store number
10040     Err_flag=1
10050     SUBEXIT
10060   END IF
10070   OUTPUT @Analyser;"N"                                 ! Clear any current error
10080   CALL Valdat
10090   OUTPUT @Analyser USING "#,K";"WI"&VAL$(Sto)&Set$ END  ! Send settings string
10100   OUTPUT @Analyser                                     ! Ensure terminator following error
10110   OUTPUT @Analyser;"RS"                                ! Read status
10120   ENTER @Analyser;Status$
10130   SELECT Status$[1,2]
10140   CASE "52","53","57","58"                             ! Check for relevant errors
10150     Err_flag=1                                         ! Set error flag
10160   CASE ELSE
10170     Err_flag=0                                         ! or clear it
10180   END SELECT
10190 SUBEND
```

Example 11 Reada

16. This routine reads a measurement trace from 6500 using ASCII block transfer into a numeric array.

Input requirements :	Series 200	HP85
ASCII read command string	Command$	C$
Output definitions :	Series 200	HP85
Measurement data array	Array (*)	A( )

Sub-program calls : NONE

The command string may be any valid 6500 ASCII block read command (RMA, SHRMB, etc.). The measurement data array should be dimensioned to 422 elements (0-421).

Note that the HP85 is unable to read ASCII block data directly into a numeric array and so a loop is used to enter each element with an appropriate IMAGE statement. This restraint significantly affects transfer times.

HP85 Sub-program

```
1000 SUB "Reada" (C$,A())
1010 COM A1
1020 OUTPUT A1 ;C$ !                          Send command to 6500
1030 FOR I=0 TO 421 !                         Enter array with loop
1040 ENTER A1 USING "#,SDD.DD,X" ; A(I)
1050 NEXT I
1060 ENTER A1 !                               Complete termination of string
1070 SUBEND
```

HP200 Sub-program

```
10000 SUB Reada(Command$,Array(*))
10010   COM /A/ @Analyser
10020   OUTPUT @Analyser;Command$             ! Send command to 6500
10030   ENTER @Analyser;Array(*)              ! Read ASCII data into array
10040 SUBEND
```

Example 12 Writea

17. This routine sends measurement data from a numeric array to 6500 using an ASCII block transfer.

Input requirements :	Series 200	HP85
ASCII block write command string	Command$	C$
Measurement data array	Array (*)	A( )

Output definitions :	Series 200	HP85
Error flag	Err_flag	E

Sub-program calls : NONE

The command string may be any valid 6500 ASCII block write command (WMA, SHWMB, etc.). The array should contain 422 data values (array base 0). The error flag is set if any error occurs during data transfer (e.g. ASCII data overflow).

As with the Reada routine the HP85 implementation requires the use of a program loop to transfer the array elements which significantly increases transfer time.

HP85 Sub-program

```
1000 SUB "Writea" (C$,A(),E)
1010 COM A1
1020 CONTROL 7,16 ; 1,NUM(",") !                    Set up EOL for ',' terminator
1030 OUTPUT A1 USING "K" ; C$&VAL$(A(0)) !          Send command and first value
1040 FOR I=1 TO 420 !                               Output values 1-420 with loop
1050 OUTPUT A1 USING "K" ; A(I)
1060 NEXT I
1070 CONTROL 7,16 ; 2,13,10 !                       Restore EOL setting
1080 OUTPUT A1 USING "K" ; A(421) !                 Output last value
1090 OUTPUT A1 !                                    Ensure termination if error
1100 OUTPUT A1 ;"RS" !                              Check for error condition
1110 ENTER A1 ; S$
1120 IF S$[1,2]<>"00" THEN E=1 ELSE E=0 !           Set or clear error flag
1130 SUBEND
```

HP200 Sub-program

```
10000 SUB Writea(Command$,Array(*),Err_flag)
10010   COM /A/ @Analyser
10020   ALLOCATE Status$[10]                        ! Temporary string for status
10030   OUTPUT @Analyser;Command$;Array(*)          ! Output command and array
10040   OUTPUT @Analyser                            ! Ensure termination if error
10050   OUTPUT @Analyser;"RS"                       ! Read status
10060   ENTER @Analyser;Status$
10070   SELECT Status$[1,2]
10080   CASE "50","51","52","53","54"               ! Check for relevant errors
10090     Err_flag=1                                ! Set error flag
10100   CASE ELSE
10110     Err_flag=0                                ! or clear it
10120   END SELECT
10130   DEALLOCATE Status$                          ! Discard status string
10140 SUBEND
```

Example 13 Readb

18. This routine reads measurement data into a string using binary block transfer.

Input requirements :	Series 200	HP85
Binary block read command string	Command$	C$
Output definitions :	Series 200	HP85
Binary measurement string	Bdata$	B$

Sub-program calls : NONE

The command string may be any valid 6500 binary block read command (RYA, SHRYB, etc.). The binary data string should be dimensioned to 846 characters. Note the use of the EOI terminator with binary data.

HP85 Sub-program

```
1000 SUB "Readb" (C$,B$)
1010 COM A1
1020 OUTPUT A1 ;C$ !                          Send command to 6500
1030 ENTER A1 USING "#%,#%K" ; B$ !           Read BINARY data into string
1040 SUBEND
```

HP200 Sub-program

```
10000 SUB Readb(Command$,Bdata$)
10010   COM /A/ @Analyser
10020   OUTPUT @Analyser;Command$             ! Send command to 6500
10030   ENTER @Analyser USING "%,-K";Bdata$   ! Read BINARY data into string
10040 SUBEND
```

Example 14 Writeb

19. This routine sends binary measurement data (usually acquired with the Readb routine) to 6500.

Input requirements :	Series 200	HP85
Binary block write command string	Command$	C$
Binary measurement data string	Bdata$	B$

Output definitions :	Series 200	HP85
Error flag	Err_flag	E

Sub-program calls : NONE

The command string may be any valid 6500 binary block write command (WYA, SHWYB, etc.). The measurement data string should contain 16-bit binary data for 422 measurements preceded by the correct block format header. The error flag is set if any error occurs during data transfer. Note the use of the EOI terminator with binary data.

HP85 Sub-program

```
1000 SUB "Writeb" (C$,B$,E)
1010 COM A1
1020 CONTROL 7,16 ; 129,NUM(B$[846,846]) !      Set up EOL for EOI on last byte
1030 OUTPUT A1 USING "K" ; C$&B$[1,845] !       Send command and data
1040 CONTROL 7,16 ; 2,13,10 !                   Restore EOL setting
1050 OUTPUT A1 !                                Ensure termination if error
1060 OUTPUT A1 ;"RS" !                          Check for error condition
1070 ENTER A1 ; S$
1080 IF S$[1,2]<>"00" THEN E=1 ELSE E=0 !       Set or clear error flag
1090 SUBEND
```

HP200 Sub-program

```
10000 SUB Writeb(Command$,Bdata$,Err_flag)
10010   COM /A/ @Analyser
10020   ALLOCATE Status$[10]                              ! Temporary string for status
10030   OUTPUT @Analyser USING "#,K";Command$&Bdata$ END  ! Output command and data
10040   OUTPUT @Analyser                                  ! Ensure termination if error
10050   OUTPUT @Analyser;"RS"                             ! Read status
10060   ENTER @Analyser;Status$
10070   SELECT Status$[1,2]
10080   CASE "51","52","53"                               ! Check for relevant errors
10090     Err_flag=1                                      ! Set error flag
10100   CASE ELSE
10110     Err_flag=0                                      ! or clear it
10120   END SELECT
10130   DEALLOCATE Status$                                ! Discard status string
10140 SUBEND
```

Example 15 Writet

20. This routine uses the TX command to position text at any location on the 6500 CRT.

Input requirements :	Series 200	HP85
X text start location	Tabx	X
Y text start location	Taby	Y
Text string	Text$	T$

Output definitions : NONE

Sub-program calls : NONE

The X location should be in the range 1-40 and the Y location should be in the range 1-24. The maximum text length will depend on the X start location but should not be more than 40 printable characters. The routine does not switch off any other display elements. This can be performed by the main program with the DA command if required.

HP85 Sub-program

```
1000 SUB "Writet" (X,Y,T$)
1010 COM A1
1020 DIM S$[80] !                                String for compilation
1030 INTEGER X1,Y1 !                             Position counters
1040 S$="TX"&CHR$(34)&CHR$(1) !                  Set up command with TP home code
1050 Y1=Y !                                      Add TP down codes
1060 IF Y1=1 THEN 1100
1070 S$=S$&CHR$(10)
1080 Y1=Y1-1
1090 GOTO 1060
1100 X1=X !                                      Add TP right codes
1110 IF X1=1 THEN 1150
1120 S$=S$&CHR$(7)
1130 X1=X1-1
1140 GOTO 1110
1150 S$=S$&T$&CHR$(34) !                         Add text and close quotes
1160 OUTPUT A1 ;S$ !                             Send complete command to 6500
1170 SUBEND
```

HP200 Sub-program

```
10000 SUB Writet(INTEGER Tabx,Taby,Text$)
10010   COM /A/ @Analyser
10020   ALLOCATE String$[80]                        ! Temporary string for compilation
10030   INTEGER Xpos,Ypos                           ! Position counters
10040   String$="TX"&CHR$(34)&CHR$(1)               ! Set up command with TP home code
10050   Ypos=Taby                                   ! Add required number of TP down codes
10060   WHILE Ypos>1
10070     String$=String$&CHR$(10)
10080     Ypos=Ypos-1
10090   END WHILE
10100   Xpos=Tabx                                   ! Add required number of TP right codes
10110   WHILE Xpos>1
10120     String$=String$&CHR$(7)
10130     Xpos=Xpos-1
10140   END WHILE
10150   String$=String$&Text$&CHR$(34)              ! Add text and close quotes
10160   OUTPUT @Analyser;String$                    ! Send complete command to 6500
10170   DEALLOCATE String$                          ! Discard compiled string
10180 SUBEND
```

Example 16 Keysrq

21. This routine sets up SRQ on front panel operation and waits for an interrupt to occur. The routine returns a numeric value indicating a key press, brightline movement or invalid SRQ condition.

Input requirements : NONE

Output definitions :	Series 200	HP85
Front panel code	see below	K

Sub-program calls : NONE

The Series 200 version of this routine is implemented as a function and should be called with :

Variable=FNKeysrq

The value returned will be in the range -1 to 40. A value of -1 indicates that the SRQ received was not generated by 6500. Values 0 to 38 represent front panel keys as defined in Appendix D. Values 39 and 40 indicate brightline left and right respectively.

HP85 Sub-program

```
1000 SUB "Keysrq" (K)
1010 COM A1
1020 K=-2 !                                            Preset code value
1030 OUTPUT A1 ;"SQ00010" !                            Set up 6500 SRQ mask
1040 ON INTR 7 GOSUB 1120 !                            Set up controller interrupts
1050 ENABLE INTR 7;8
1060 IF K<>-2 THEN 1080 !                              Wait for valid code
1070 GOTO 1060
1080 OUTPUT A1 ;"SQ00000" !                            Disable 6500 SRQ
1090 OFF INTR 7 !                                      and controller interrupts
1100 SUBEXIT !                                         Exit with code
1110 ! ----------------------------------------------- SRQ service routine
1120 STATUS 7,1 ; S !                                  Reset interface interrupt
1130 S=SPOLL(A1) !                                     Fetch status byte from 6500
1140 IF NOT BIT(S,6) THEN K=-1 @ RETURN !              Check SRQ active
1150 S=S-64 !                                          Mask SRQ bit
1160 IF S<>1 THEN 1200
1170 OUTPUT A1 ;"RK" !                                 If key-press
1180 ENTER A1 ; K !                                    Read key code
1190 RETURN !                                          and return
1200 IF S=2 THEN K=39 @ RETURN !                       If BL left set code=39
1210 IF S=3 THEN K=40 @ RETURN !                       If BL right set K=40
1220 K=-1 !                                            This should never occur
1230 RETURN
1240 SUBEND
```

HP200 Sub-program

```
10000 DEF FNKeysrq
10010   COM /A/ @Analyser
10020   Code=-2                                                ! Preset code value
10030   OUTPUT @Analyser;"SQ00010"                             ! Set up 6500 SRQ mask
10040   ON INTR 7 GOSUB Service                                ! Set up controller interrupts
10050   ENABLE INTR 7;2
10060   WHILE Code=-2                                          ! Wait for valid code
10070   END WHILE
10080   OUTPUT @Analyser;"SQ00000"                             ! Disable 6500 SRQ
10090   OFF INTR 7                                             ! and controller interrupts
10100   RETURN Code                                            ! Exit with code
10110 !--------------------------------------------------------!
10120 Service:                                                 ! SRQ service routine
10130 !--------------------------------------------------------!
10140   Sbyte=SPOLL(@Analyser)                                 ! Fetch status byte from 6500
10150   IF NOT BIT(Sbyte,6) THEN                               ! Check SRQ active
10160     Code=-1                                              ! Indicate no SRQ with negative code
10170     RETURN
10180   END IF
10190   Sbyte=Sbyte-64                                         ! Mask SRQ bit
10200   SELECT Sbyte                                           ! Examine status byte
10210   CASE 1                                                 ! If key-press fetch key code
10220     OUTPUT @Analyser;"RK"
10230     ENTER @Analyser;Code
10240   CASE 2                                                 ! If BL left set code=39
10250     Code=39
10260   CASE 3                                                 ! If BL right set code=40
10270     Code=40
10280   CASE ELSE                                              ! This should never occur
10290     Code=-1
10300   END SELECT
10310   RETURN
10320 FNEND
```

Example 17 Plocal

22. This routine implements a 'pseudo-local' mode of operation where the instrument appears to be operating under local control, but is in face under remote control. This is achieved by intercepting all front panel operations with SRQ interrupts and simulating the operations performed with GPIB commands. The routine illustrates the use of the XK command. A key code value is supplied to the routine which is used as an exit code. For example if the value 16 was supplied control would revert to the main program when the LOCAL key was pressed. A status code is returned indicating exit due to a non-6500 interrupt.

23. A square block is written to the top left of the CRT to indicate 'pseudo-local' operation. When the exit code is recognized a housekeeping routine is performed to ensure that the instrument is left in a predictable state. In some cases the exit procedure involves waiting for valid data or the end of a plot function. During this waiting period the indicator is caused to flash. The indicator is removed on leaving the routine.

24. Due to speed limitations an HP85 version of this routine is not presented, although it is technically feasible to implement.

Input requirements :	Series 200
Exit code	Exit_code
Output definitions :	Series 200
Status code (0=normal, 1=non-6500 SRQ)	Exit_status

Sub-program calls : NONE

The Exit code should be in the range 0-38 and represents a key code as defined in Appendix D.

25. This routine is not intended to be a solution to any specific system requirement but illustrates the extent to which the front panel SRQ facility may be used. Many useful additions could be made to the routine. Here are some examples :

Sending previously acquired normalization data when frequency limits are changed.

Switching off RF power when AUTO ZERO is pressed.

Performing automatic digital plots when PLOT is pressed.

Modifying CRT annotation.

Adding extra operator prompts and instructions.

Implementing 'menu' operation.

HP200 Sub-program

```
10000 SUB Plocal(Exit_code,Exit_status)
10010   COM /A/ @Analyser
10020   ALLOCATE Status$[24]                                ! Temporary string for status
10030   INTEGER Sh_flag                                      ! Shift key flag
10040   Indic$="TX"&CHR$(34)&CHR$(1)&CHR$(127)&CHR$(34)     ! TX string for mode indicator
10050   Exit$=Indic$                                         ! TX string for exit indicator
10060   Exit$[5,5]=CHR$(255)
10070   Remov$=Indic$                                        ! TX string to remove indicator
10080   Remov$[5,5]=" "
10090   OUTPUT @Analyser;"SQ00010"                           ! Set up 6500 SRQ mask
10100   OUTPUT @Analyser;Indic$                              ! Display indicator
10110   Sh_flag=0                                            ! Pre-set shift flag
10120   !----------------------------------------------------!
10130   LOOP                                                 ! MAIN LOOP
10140     GOSUB Fetch_key                                    ! Fetch key code
10150   EXIT IF Key_code=Exit_code OR Key_code=-1            ! Leave if EXIT key pressed or non-6500 SRQ
10160     SELECT Key_code                                    ! Examine key code
10170     CASE -1
10180       Command$="0"                                     ! Dummy command if not 6500 SRQ
10190     CASE 20
10200       Sh_flag=NOT Sh_flag                              ! Toggle shift flag
10210       Command$="SH"
10220     CASE ELSE
10230       Command$="XK"                                    ! Execute all other keys
10240     END SELECT
10250     IF Sh_flag AND Command$<>"SH" THEN
10260       Command$="SH"&Command$                           ! Ensure correct SHIFT operation
10270     END IF
10280     OUTPUT @Analyser USING "#,K";Command$              ! Send command to 6500
10290     OUTPUT @Analyser;Indic$                            ! Re-write indicator
10300     IF Sh_flag THEN                                    ! Shift flag set contingency
10310       IF Command$<>"SH" THEN                           ! Commands reset SHIFT state
10320         Sh_flag=0
10330       ELSE
10340         OUTPUT @Analyser USING "#,K";"SH"              ! Send SHIFT to retain mode
10350       END IF
10360     END IF
10370   END LOOP
10380   !----------------------------------------------------! EXIT housekeeping.......
10390   OUTPUT @Analyser;Exit$                               ! Change to flashing indicator
10400   OUTPUT @Analyser;"RX"
10410   ENTER @Analyser;Status$                              ! Read status
10420   IF Status$[11,11]="7" OR Status$[14,14]="1" THEN     ! If in CALAID or PLOT menu
10430     OUTPUT @Analyser;"N"                               ! Clear with NORMAL
10440   ELSE
10450     IF Status$[14,14]="2" THEN                         ! If PLOT routine active
10460       REPEAT                                           ! wait until finished
10470         WAIT .1
10480         OUTPUT @Analyser;"RX"
10490         ENTER @Analyser;Status$
10500       UNTIL Status$[14,14]="1"
10510       OUTPUT @Analyser;"N"                             ! Clear with normal
10520     ELSE
10530       IF Status$[5,5]="0" THEN                         ! Wait for valid data
10540         REPEAT
10550           WAIT .1
10560           OUTPUT @Analyser;"RX"
10570           ENTER @Analyser;Status$
10580         UNTIL Status$[5,5]="1"
10590       END IF
```

HP200 Sub-program 2

```
10600        IF Status$[8,8]="0" THEN                          ! If not in FREEZE
10610          IF Status$[10,10]="M" THEN                      ! Check for MEMORY display
10620            OUTPUT @Analyser;"N"                          ! Clear with NORMAL
10630          ELSE
10640            OUTPUT @Analyser;"FZFZ"                       ! Prompts cleared by toggling FREEZE
10650          END IF
10660        END IF
10670      END IF
10680    END IF
10690    OUTPUT @Analyser;"SQ00000"                            ! Reset 6500 SRQ mask
10700    OUTPUT @Analyser;Remov$                               ! Remove indicator
10710    DEALLOCATE Status$                                    ! Discard status
10720    IF Key_code=-1 THEN                                   ! Set EXIT status
10730      Exit_status=1
10740    ELSE
10750      Exit_status=0
10760    END IF
10770    SUBEXIT                                               ! Exit from routine
10780 !-------------------------------------------------------!
10790 Fetch_key:                                               ! Keyboard control routine
10800 !-------------------------------------------------------!
10810    Key_code=-2                                           ! Preset key code
10820    ON INTR 7 GOSUB Service                               ! Set up controller interrupts
10830    ENABLE INTR 7;2
10840    WHILE Key_code=-2                                     ! Wait for valid key code
10850    END WHILE
10860    OFF INTR 7                                            ! Disable interrupts
10870    RETURN                                                ! Return with key code
10880 !-------------------------------------------------------!
10890 Service:                                                 ! SRQ service routine
10900 !-------------------------------------------------------!
10910    Sbyte=SPOLL(@Analyser)                                ! Fetch 6500 status byte
10920    Sbyte=Sbyte-64                                        ! Mask SRQ bit
10930    SELECT Sbyte                                          ! Examine status byte
10940    CASE 1                                                ! If key press
10950      OUTPUT @Analyser USING "#,K";"RK"                   ! Read key code
10960      ENTER @Analyser;Key_code
10970    CASE 2                                                ! If brightline left
10980      GOSUB Read_pos                                      ! Find current position
10990      IF Blpos>0 THEN OUTPUT @Analyser USING "#,K";"BL"   ! Execute BL if valid
11000      IF Sh_flag THEN OUTPUT @Analyser USING "#,K";"SH"   ! Re-assert SHIFT if necessary
11010    CASE 3                                                ! If brightline right
11020      GOSUB Read_pos                                      ! Find current position
11030      IF Blpos<421 THEN OUTPUT @Analyser USING "#,K";"BR" ! Execute BR if valid
11040      IF Sh_flag THEN OUTPUT @Analyser USING "#,K";"SH"   ! Re-assert SHIFT if necessary
11050    CASE ELSE                                             ! If non-6500 SRQ
11060      Key_code=-1                                         ! Return invalid KEY_CODE
11070    END SELECT
11080    IF Key_code<>-1 THEN ENABLE INTR 7                    ! Re-enable interrupts if valid key_code
11090    RETURN                                                ! and return
11100 !-------------------------------------------------------!
11110 Read_pos:                                                ! Read current brightline position
11120 !-------------------------------------------------------!
11130    OUTPUT @Analyser USING "#,K";"RP"
11140    ENTER @Analyser;Blpos
11150    RETURN
11160 SUBEND
```

Binary/ASCII conversions

27. The binary and ASCII measurement transfers illustrated in examples 11-14 have different areas of application, but it may be desirable in some cases to convert from one format to the other. Two routines are presented which perform these conversions and will run on both the HP Series 200 and the HP85 computers.

The first example illustrates conversion from binary to ASCII. Previously acquired binary data is assumed to be in the string B$ and the target array is A which must be dimensioned with 422 elements (base 0).

The second example illustrates conversion from ASCII to binary. Previously acquired or generated ASCII data is assumed to be in the array A and the target string is B$ which must be dimensioned with 846 characters.

Essentially the routines are manipulations in 2's complement arithmetic. Note, however, that the sign bit is 0 for a negative value in 6500 internal format.

Binary string to numeric array conversion

```
1000 FOR I=0 TO 421
1010   M=NUM(B$[I*2+4,I*2+4])
1020   L=NUM(B$[I*2+3,I*2+3])
1030   N=L+M*256
1040   IF N>32767 THEN N=N-65536
1050   A(I)=-N/256
1060 NEXT I
```

Numeric array to binary string conversion

```
1000 B$="#I"
1010 FOR I=0 TO 421
1020   N=-INT(A(I)*256+.5)
1030   IF N<0 THEN N=N+65536
1040   M=N DIV 256
1050   L=N MOD 256
1060   B$=B$&CHR$(L)&CHR$(M)
1070 NEXT I
```

Appendix A

6500 FIRMWARE* ISSUE 5 AND PRE ISSUE 5 COMPARISON

1. The dB REL commands (SH8 and SH9) now require the E terminator following an optional numeric argument. With pre-issue 5 versions these commands did not use any arguments.

2. The brightline frequency value output following the RF command is now in GHz rather than Hz. This gives compatibility with the frequency input commands, which all assume GHz units.

3. The brightline amplitude values output following the RA, RB, or RR commands are now rounded to two decimal places. With pre-issue 5 versions three decimal places were output, despite the resolution limitation of 1/256 dB.

4. The interpretation of bits 0-3 of the serial poll status byte has changed. With pre-issue 5 versions decimal values of 1-9 were interpreted as numeric key presses 1-9. The new interpretation (see SRQ FACILITIES - section 32) coupled with the RK command allows SRQ interrupts on any key press or brightline movement.

5. The following commands are not available with pre-issue 5 versions :

RMA	RMB	RMR	RYA	RYB	RYR
SHRMA	SHRMB	SHRMR	SHRYA	SHRYB	SHRYR
WMA	WMB	WMR	WYA	WYB	WYR
SHWMA	SHWMB	SHWMR	SHWYA	SHWYB	SHWYR
RDA	RDB	RDR	RDF	RI	WI
RX	RMK	RP	RK	XK	DA
TX	DPA	DPB	DPG	DPL	

*Firmware is the term given to the instrument's internally fixed operating system.

Appendix B

GPIB ERROR CODES

Code	*Meaning*
31	Attempt to move brightline outside valid area (positions 0-421) using the BL, BR or BP commands.
50*	ASCII data in WM transfer outside valid range (+/-99.99).
51*	Format error - illegal character in WM ASCII transfer data string.
52*	Premature termination of WY, WM or WI transfer.
53*	No termination of WY, WM or WI transfer.
54*	Listen buffer overflow (may be caused by absence of separators between ASCII values in WM transfer).
55	Argument to RI or WI command outside valid range (1-9).
56	Attempt to read from a 'null' store with RI.
57*	Format error on WI transfer block header.
58*	Checksum error on WI transfer.
60	Attempt to read an HPGL plotter control string (DPA, DPB, DPG or DPL commands) when in CALAID mode.

*These commands cause the operation to be aborted until receipt of a valid SR2/3 terminator [CR]LF or EOI. See IEEE 728-1982 for full definition of terminators.

Appendix C

6500 CHARACTER SET AND TEXT CONTROL CODES

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1	Γ	[illegible]	Δ	δ	ε	λ	μ	π	ρ	Σ	σ	Φ	Ω	[illegible]	∠	[illegible]
2		!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_
6	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z	{	|	}	~	█

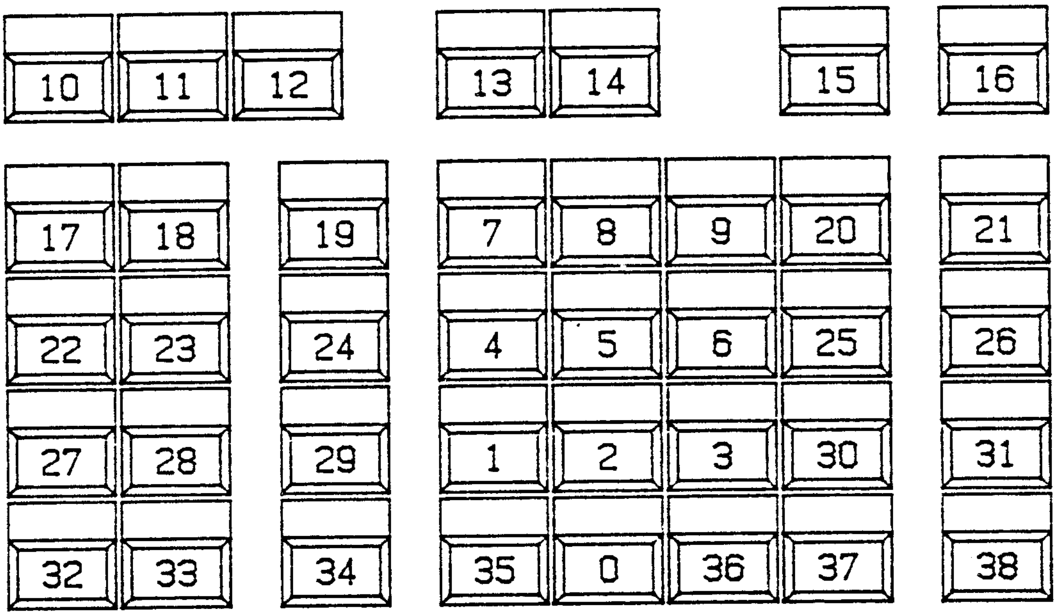
CONTROL CODES

Character codes 0 to 15 are not displayed but are used as control codes in the following manner :

Code	Function (TP = Text Pointer)
0	Ignored.
1	Move TP to top left of screen (Row 1, Column 1).
2	Clear current row and move TP to column 1.
3	Clear text from TP to end of current row.
4	Set TAB at current TP column.
5	Reset TAB at current TP column.
6	Clear all tabs.
7	Move TP one position right unless at column 40.
8	Move TP one position left unless at column 1.
9	Move TP to next TAB position or column 40.
10	Move TP one position down unless on row 24.
11	Move TP one position up unless on row 1.
12	Clear all text and move TP to top left of screen.
13	Move TP to column 1 of current row.
14	Enable flash mode for subsequent characters.
15	Disable flash mode.

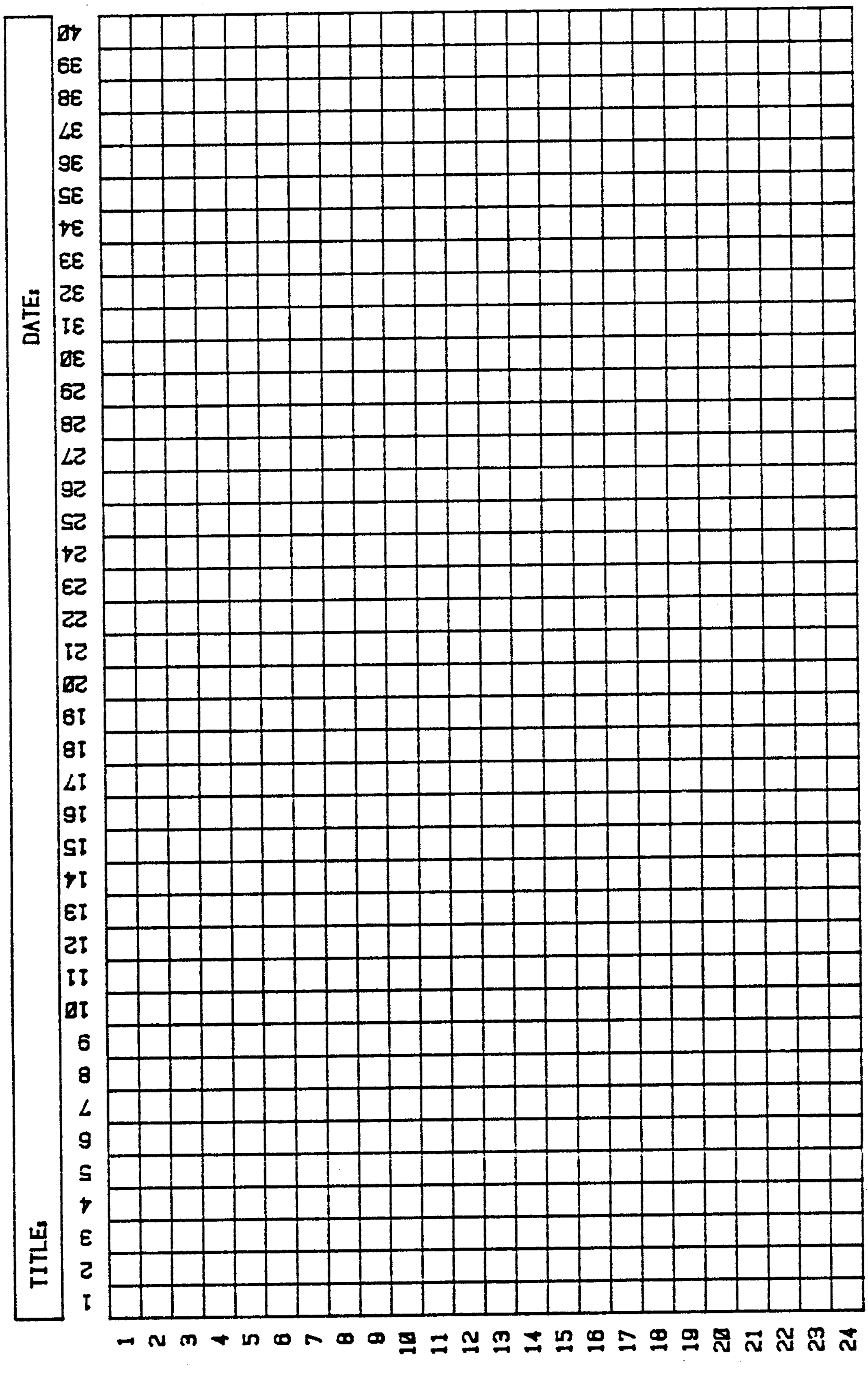
Appendix D

KEYBOARD CODES RETURNED BY RK COMMAND



Appendix E

6500 CRT LAYOUT CHART



Appendix F

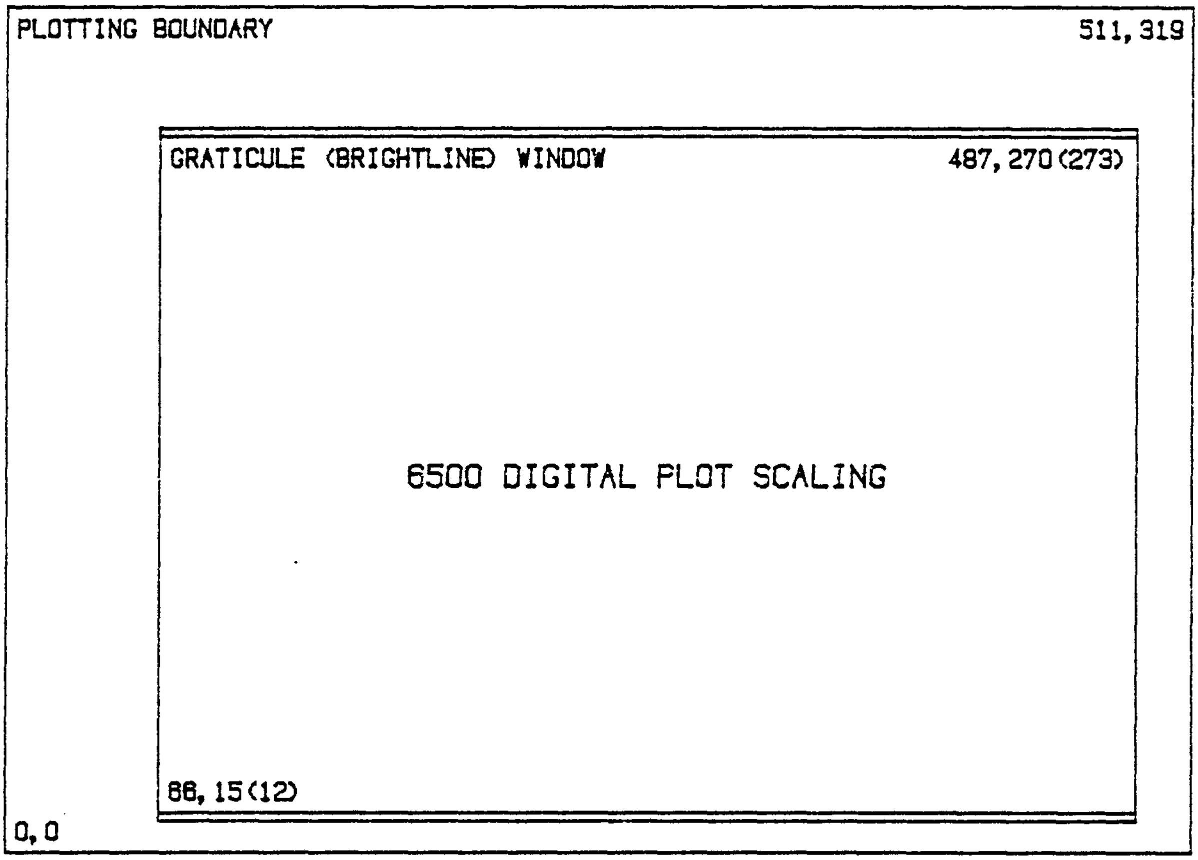
STANDARD ALPHANUMERIC LAYOUTS
FOR SINGLE AND DUAL CHANNEL DISPLAYS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
1							P	o	w	e	r																								1	0	0	m	s	
2		d	B	m			A	=	●	n	n	.	n	n		d	B	m																	S	w	e	e	p	
3	●	n	n	.	n																																			
4																																								
5	●	n	n	.	n																																			
6																																								
7	●	n	n	.	n																																			
8																																								
9	●	n	n	.	n																																			
10																																								
11	●	n	n	.	n																																			
12																																								
13	●	n	n	.	n																																			
14																																								
15	●	n	n	.	n																																			
16																																								
17	●	n	n	.	n																																			
18																																								
19	●	n	n	.	n																																			
20																																								
21	●	n	n	.	n																																			
22																																								
23	●	n	n	.	n																																			
24								n	n	.	n	n		F	r	e	q	u	e	n	c	y		n	n	.	n	n		G	H	z			n	n	.	n	n	

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
1							P	o	w	e	r																								1	0	0	m	s	
2		d	B	m			A	=	●	n	n	.	n	n		B	=	●	n	n	.	n	n		d	B	m								S	w	e	e	p	
3	●	n	n	.	n																																			
4	●	n	n	.	n																																			
5																																								
6																																								
7	●	n	n	.	n																																			
8	●	n	n	.	n																																			
9																																								
10																																								
11	●	n	n	.	n																																			
12	●	n	n	.	n																																			
13																																								
14																																								
15	●	n	n	.	n																																			
16	●	n	n	.	n																																			
17																																								
18																																								
19	●	n	n	.	n																																			
20	●	n	n	.	n																																			
21																																								
22																																								
23	●	n	n	.	n																																			
24	●	n	n	.	n			n	n	.	n	n		F	r	e	q	u	e	n	c	y		n	n	.	n	n		G	H	z			n	n	.	n	n	

Appendix G

DIGITAL PLOTTER OUTPUT INFORMATION



The plotting area is scaled as 512 x 320 user units.

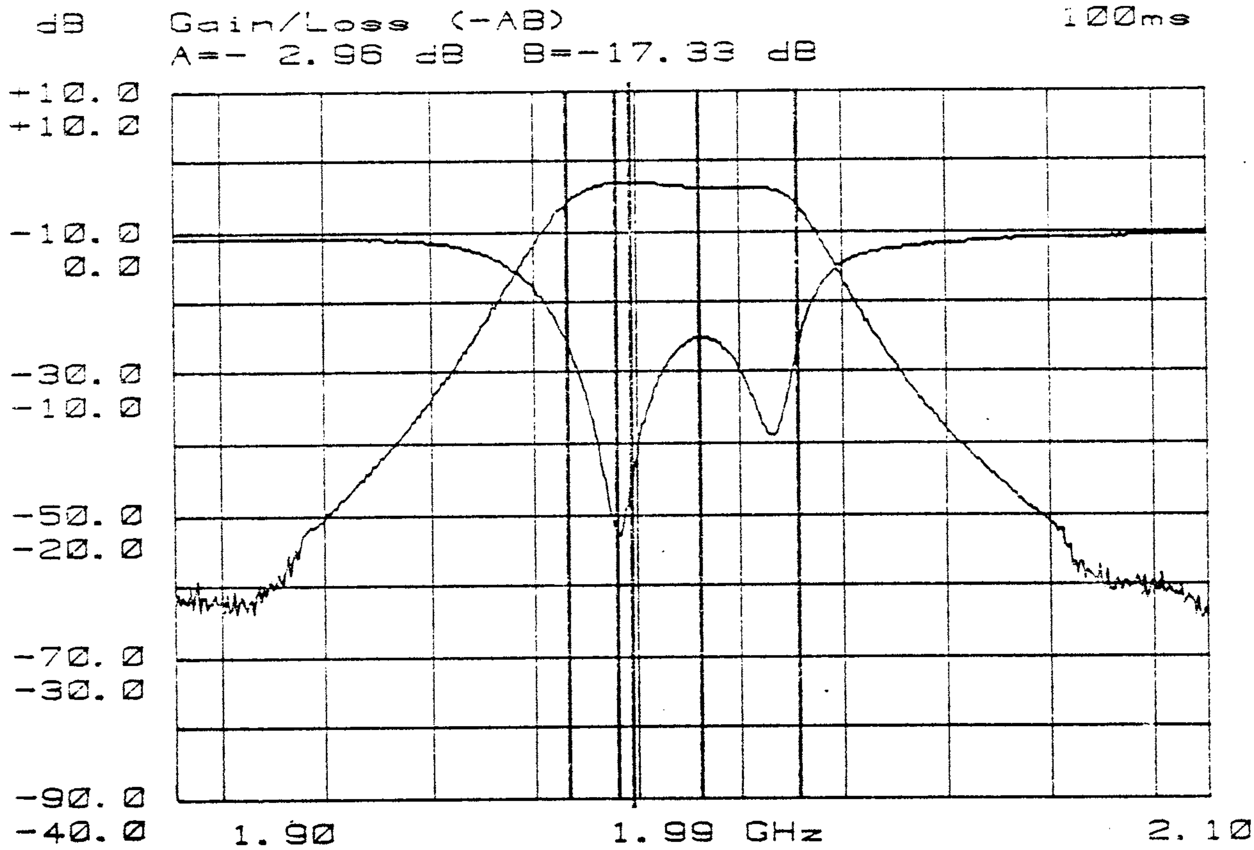
The character size is set to: 1.456% of vertical scale
2.000% of horizontal scale.

Starting co-ordinates of labels:

Units	0,293	
Sweep Speed	429,293	
Start Frequency	66, 0	
Brightline Frequency	221, 0	
Stop Frequency	440, 0	
Datum 1	0,268	
Datum 2	0,256	(Dual channel only)
Top Line	66,293	
Second Line	66,281	

Appendix H

SAMPLE DIGITAL PLOT



EQUIPMENT 6500

TITLE .... Automatic amplitude analyzer

EARLIER CHANGES
APPLICABLE ..... None

MANUAL CHANGE

To improve noise immunity and common mode rejection of the signal channel, capacitor C37 (100pF) on AC12 is no longer fitted. Disregard references to C37 in the parts list (Chap. 6, para. 15) and on the circuit diagram (Chap. 7, Fig. 8).

Service Manual
H 6500
Vol. 2

AUTOMATIC AMPLITUDE ANALYSER

6500

Including Option 6500-001 (GPIB Interface)

AMENDMENT RECORD

The following amendments are incorporated in this manual.

Amendment No.	Date	Issued at Ser. No.
Commencing	Jan. 83	100
Am. 1	Aug. 83	265
Am. 2	Jun. 84	365
Am. 3	Feb. 86	540
Am. 4	May 87	664

Part No. 46881-559W
Print code F - 11/87, MI 0.35c

CONTENTS

PRELIMINARIES

CHAPTERS

HAZARD WARNING SYMBOLS

The following symbols appear on the equipment :

Symbol	Type of hazard	Reference in manual
⚠	Static sensitive device	Vol. 2 Page (iv)
⚠	Dangerous voltage present	Vol. 2 Page (iii)
⚠	Supply voltage	Vol. 2 Page (iii)

Note ...

Each page bears the date of the original issue or the code number and date of the latest amendment (Am. 1, Am. 2 etc.). New or amended material of technical importance introduced by the latest amendment is indicated by triangles positioned thus ▶ ..... ◀ to show the extent of the change. When a chapter is reissued the triangles do not appear. Any changes subsequent to the latest amendment state of the manual are included on inserted sheets coded C1, C2 etc.

NOTES AND CAUTIONS

ELECTRICAL SAFETY PRECAUTIONS

This equipment is protected in accordance with IEC Safety Class 1. It has been designed and tested according to IEC Publication 348, 'Safety Requirements for Electronic Measuring Apparatus', and has been supplied in a safe condition. The following precautions must be observed by the user to ensure safe operation and to retain the equipment in a safe condition.

Defects and abnormal stresses

Whenever it is likely that protection has been impaired, for example as a result of damage caused by severe conditions of transport or storage, the equipment shall be made inoperative and be secured against any unintended operation.

Removal of covers

⚠ Removal of the covers is likely to expose live parts although reasonable precautions have been taken in the design of the equipment to shield such parts. The equipment shall be disconnected from the supply before carrying out any adjustment, replacement or maintenance and repair during which the equipment shall be opened. If any adjustment, maintenance or repair under voltage is inevitable it shall only be carried out by a skilled person who is aware of the hazard involved.

Note that capacitors inside the equipment may still be charged when the equipment has been disconnected from the supply. Before carrying out any work inside the equipment, capacitors connected to high voltage points should be discharged; to discharge mains filter capacitors, if fitted, short together the L (live) and N (neutral) pins of the mains plug.

⚠ Note also that the 12 kV e.h.t. circuit for the cathode ray tube retains its charge for a considerable time after switch off. Therefore before any handling is carried out in the vicinity of the cathode ray tube or e.h.t. unit it is essential that the supply is disconnected from the instrument and the final anode lead is shorted to the chassis several times immediately after unplugging. The residual charge on the c.r.t. itself must also be removed by shorting the anode connection to earth.

Mains plug

The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action shall not be negated by the use of an extension lead without protective conductor. Any interruption of the protective conductor inside or outside the equipment is likely to make the equipment dangerous.

Primary fuses

⚠ Note that there is a supply fuse in both the live and neutral wires of the supply lead. If only one of these fuses should rupture, certain parts of the equipment could remain at supply potential.

To provide protection against breakdown of the supply lead, its connectors, and filter where fitted, an external supply fuse (e.g. fitted in the connecting plug) should be used in the live lead. The fuse should have a continuous rating not exceeding 6 A.

Make sure that only fuses with the required rated current and of the specified type are used for replacement. The use of mended fuses and the short-circuiting of fuse holders shall be avoided.

Secondary fuses

Each secondary winding of transformer T1 (with the exception of +5 V and +12 V supply lines, adequately protected by the primary fuses F1 and F2) is fused with a 250 mA, A-T (250 milliamp time lag) fuse to provide added safety. These are situated on the secondary tag board within the instrument and can be accessed by removing the lower cover.

CAUTION : STATIC SENSITIVE COMPONENTS

Components identified with the symbol ⚠ on the circuit diagrams and/or parts lists are static sensitive devices. The presence of such devices is also indicated in the equipment by orange discs, flags or labels bearing the same symbol. Certain handling precautions must be observed to prevent these components being permanently damaged by static charges or fast surges.

(1) If a printed board containing static sensitive components (as indicated by a warning disc or flag) is removed, it must be temporarily stored in a conductive plastic bag.

(2) If a static sensitive component is to be removed or replaced the following anti-static equipment must be used.

A work bench with an earthed conductive surface.

Metallic tools earthed either permanently or by repeated discharges.

A low-voltage earthed soldering iron.

An earthed wrist strap and a conductive earthed seat cover for the operator, whose outer clothing must not be of man-made fibre.

(3) As a general precaution, avoid touching the leads of a static sensitive component. When handling a new one, leave it in its conducting mount until it is required for use.

(4) If using a freezer aerosol in fault finding, take care not to spray programmable ICs as this may affect their contents.

WARNING : HANDLING HAZARDS

This equipment is formed from metal pressings and although every endeavour has been made to remove sharp points and edges, care should be taken, particularly when servicing the equipment, to avoid minor cuts.

When exposing or handling the cathode ray tube care must be taken to prevent implosion and possible scattering of glass fragments.
Handling should only be carried out by experienced personnel and the use of safety mask and gloves is recommended.
A defective tube should be disposed of in a safe manner by an authorized waste contractor.

WARNING : TOXIC HAZARD

Many of the electronic components used in this equipment employ resins and other chemicals which give off toxic fumes on incineration. Appropriate precautions should therefore be taken in the disposal of these items.

Chapter 4

TECHNICAL DESCRIPTION

CONTENTS

INTRODUCTION

1. The 6500 Automatic Amplitude Analyser is a microprocessor controlled scalar network analyser. When used in conjunction with an r.f. sweeper, the instrument facilitates the measurement of transmission loss or gain, return loss or power, the results being displayed in graphical form on the integral CRT.

BRIEF OVERALL DESCRIPTION

2. The 6500 has 3 independent channels, to which are connected detectors, each has a data store which holds 'live' measurement data and an associated memory for holding reference data for normalisation purposes. Each memory and data store can hold a complete sweep of 422 measurement points across the selected frequency range. The 3 input channels are multiplexed and before a sweep is started the required channel is switched on. At each measurement point the microprocessor accesses from the signal processing stages a log converted value of the signal and stores it in the channel data store. This data is converted into a displayed value using the screen parameters of DATUM and RANGE.

3. Keyboard selection allows live displays of channels A,B and R independently or a combined display of channels A and B. The associated memories are used to store the system response before insertion of the device-under-test. The appropriate memory is then subtracted from the live display to give a normalized response. Channel R (the reference channel) is used in parallel with the measurement channels (A and B) to prevent any variation in the sweeper's output from affecting the response obtained for the device-under-test.

4. The AUTO key enables the optimum screen display of the amplitude of the required channel(s) to be shown. Vertical graticule lines are placed automatically.

5. RANGE and DATUM keys enable the amplitude display to be varied. LIMITS may be set for amplitude maximum or minimum and if exceeded an error message is displayed, or an SRQ command sent via the GPIOtB (if this option is fitted).

6. All front panel functions may be controlled via the GPIB interface, if this option is fitted. The interface is available either factory-fitted or as an optional accessory for field-installation. The interface conforms to the IEEE 488 standard, but an accessory is available to convert to IEC 625 systems.

7. An automatic self test routine is carried out when the instrument is switched on and a ZERO facility exists to enable stray system voltages on each of the 3 channels to be compensated for.

8. Channels may be displayed as either a LINE or HISTOGRAM for ease of viewing. The display may be frozen for photography or output to hard copy via the PLOT facility.

9. A BRIGHTLINE is shown vertically on the display giving a readout of amplitude and frequency to 0.01 dB and 10 MHz resolution. It can be set to MAX or MIN values or used to set up frequency bands for measurement or to zoom-in on an item of interest on screen. The BRIGHTLINE is also used for displaying up to 8 on-screen markers and has a ΔF function, allowing the sweep to be centred on the brightline position. This is particularly useful for filter analysis.

10. The PLOT facility drives a standard X-Y recorder and prints the displayed amplitude and frequency details shown on screen. A menu allows a choice of axes annotated for frequency and amplitude scales, and selects the speed of plotting for accurate results to be recorded.

11. Low noise detectors in the 6500 series maintain a high accuracy. True square law and temperature correction is provided up to +16 dBm for high power measurements without compression. The 6500 has a dynamic range of 66 dB in normal operation. An AVERAGE facility can reduce the noise level to -55 dBm.

12. Amplitude scaling in dB, dBm, mW or VSWR and user selected limits, (High, Low, Channels A and B) may be programmed and stored via the keyboard. Messages are also flashed on screen when limits are exceeded. The STATUS function displays: the current user parameters, their status (enabled or disabled), current GPIB address, frequency range and dB relative values.

13. Up to 9 such front panel settings may be stored and recalled. The frequency scaling on the X axis and BRIGHTLINE may be removed for security (when photographing the display for example) using the SECRET key. Calibration aid is provided and the 6500 has many self diagnostic routines for fault finding.

BRIEF UNIT TECHNICAL DESCRIPTION

14. The 6500 is designed around a central microprocessor which exercises control and timing over the various functional blocks of the instrument. It also ensures maximum flexibility and, if required, allows programming by the General Purpose Interface Bus (GPIB). This facility is offered either built-in or as an Optional accessory.

15. The instrument is divided into five main areas see Fig. 1, these are as follows :-

(1) Power supply
(2) CRT and Display drive
(3) Display
(4) Microprocessor
(5) Signal channel and analogue interfaces

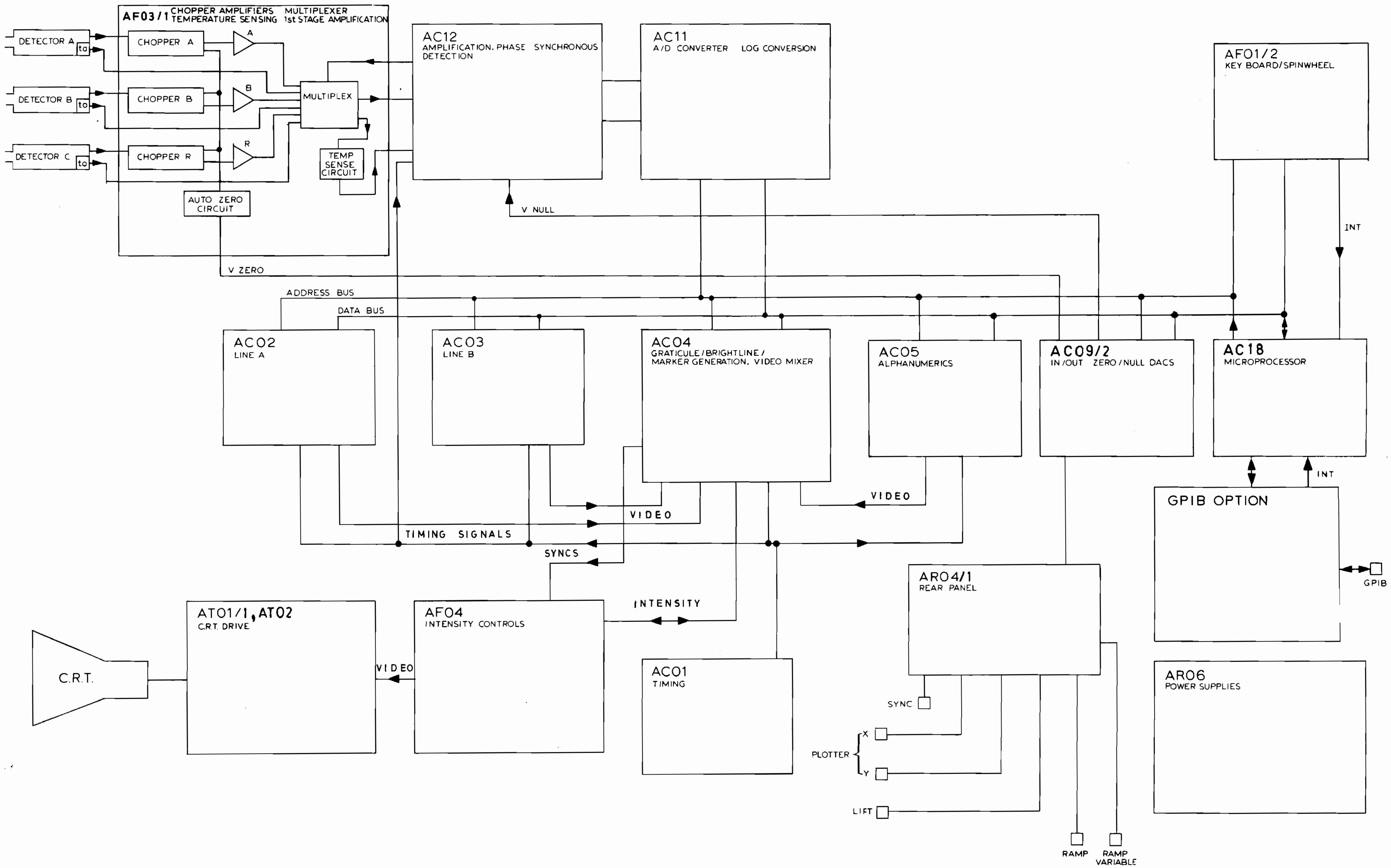


Fig. 1 6500 Amplitude Analyser, simplified block diagram

The display circuits provide timing control and access to the layers making up the overall display, and they function independently of the microprocessor so as to provide a stable display. Interfacing to the CRT/Display drive is carried out by separate sync. and video signals virtually identical to standard television signals. Generation of the e.h.t., amplification of the video signal and the power drive to the c.r.t. yoke coils are also carried out by the display (AT01/1).

16. The display drive incorporates the alphanumerics (AC05), two displays A, B in line or histogram form (AC02, AC03), and the graticule/brightline markers (AC04/1). The microprocessor is actually halted when a "Memory" display is show, thus demonstrating that the display can function without microprocessor intervention. Although most operations are performed using the microprocessor it is important (for reasons of speed) to display the information directly. Only updates of information are therefore controlled by the microprocessor.

17. All the information for the display is stored digitally in RAM memory store. This is accessed via counters synchronized to the line frequency, (line being the rate at which the electron beam in the c.r.t. is swept across the screen i.e. 15.625 kHz). In order for this information to be updated, it is necessary to provide the microprocessor with access to the RAM and this is carried out by data selectors, disconnecting the counters and allowing the RAM to be accessed by the microprocessor's address and data bus lines.

18. Each block of RAM has its own memory location in the Memory map. Addresses 8000H - 8FFFH are reserved for control ports to provide access to other functional blocks.

19. The operation of the instrument relies on standard microprocessor technology and employs an 8085A-2 (AC18) 8-bit microprocessor. It operates at a clock frequency of 5 MHz derived from a 10 MHz crystal standard. The signal channel and analogue interface form the data acquisition and plotter interface. The plotter is in fact an extension of the normal operation of the instrument, and because the plot is not required simultaneously with swept operation it uses many of the interface functions normally employed in data acquisition. e.g. The digital-analogue converter providing the plotter Y output is also used for generating the ZERO voltage.

20. Other circuits within the data acquisition block are the signal channel (AC12, AF03/1), analogue-digital converter and log conversion (AC11), port control (AC09/2) and the keyboard and spinwheel control (AF01/AF02). Each of these circuits cannot usefully function without frequent microprocessor intervention. The remainder of the instrument (excepting the c.r.t. display etc.) relies totally on the internal software program.

21. Each circuit or function is accessed via a microprocessor port. Each port has its own address, a READ port is one which provides data for the 6500 from an external source or key press. A WRITE port controls a circuit or provides an output from the 6500 e.g. Range selection or X Ramp control. Each port can be referred to by name as shown in Fig. 2.

SET GAIN (8804H)	8880H
ADC STATUS (8803H)	
ADC PORT MSB (8802H)	
ADC PORT LSB (8801H)	8800H
	8780H
	8700H
	8680H
	8600H
	8580H
	8500H
NULL DAC O/P, SYNC IN (8407H)	
GPIB SWITCH PORT (8406H)	
PLOTTER CONTROL PORT (8405H)	
PLOTTER Y DAC (8404H)	8480H
RAMP DAC ENABLE REGISTER (8403H)	
RAMP DAC BITS 8-11 (8402H)	
RAMP DAC BITS 4-7 (8401H)	
RAMP DAC BITS 0-3 (8400H)	
	8400H
	8380H
ZERO DAC ENABLE REGISTER (8207H)	
ZERO DAC BITS 8-11 (8206H)	8300H
ZERO DAC BITS 4-7 (8205H)	
ZERO DAC BITS 0-3 (8204H)	8280H
BLANKING PORT (8202H)	
DISPLAY CONTROL SWITCH (8200H)	
	8200H
ADDRESS 1/END OF SEQUENCE (8107H)	
ADDRESS 0, ADDRESS 0/1 (8106H)	
CMD PASS THROUGH/AUX MODE (8105H)	
ADDRESS STATUS MODE (8104H)	
SERIAL POLE STATUS MODE (8103H)	8180H
INTERRUPT STATUS/MASK 2 (8102H	
INTERRUPT STATUS/MASK 1 (8101H)	
GPIB DATA 1/0 (8100H)	
	8100H
FRONT PANEL LED PORT (8084H)	
RESET INTERRUPTS (8083H)	
SPINWHEEL DATA (8082H)	
INTERRUPT STATUS DATA (8081H)	
KEYBOARD DATA PORT (8080H)	8080H
	8000H

Fig. 2 Memory mapped ports

22. The three input channels A, B and R each have an f.e.t. chopper (parts of AF03/1) immediately following the input socket to give a low noise input. After the first stage of amplification Ax1 or Ax100 gain, which is controlled by the microprocessor, signals are multiplexed or switched from A,B or R channels to a single signal path. This is buffered and fed via an SMA connector to the Signal board (AC12) where two further stages of gain (microprocessor controlled) are available to provide a signal level of approximately 2 V.

23. On AC12 the signal is fed initially to a simple sample and hold (de-glitch) circuit to remove noise spikes generated by the chopper which at low levels are far greater than the signal itself (40-100 mV spikes may be present at the chopper which must discern signals as small as 1 μV). After the third amplifier stage the signal is restored to a d.c. level by a phase synchronous detector and a d.c. amplifier where a programmable offset voltage is added to null any shape changes that occur on the different ranges.

24. The d.c. signal is finally passed through a switch (where a temperature correction signal can be selected) and clipped to prevent negative-going transitions which would otherwise damage the following A-D converter. The overall gain is controlled (in six ranges) by the microprocessor as is the switching through of the required channel and temperature sensor, see Fig. 3.

Signal channel (AF03/1,AC12)

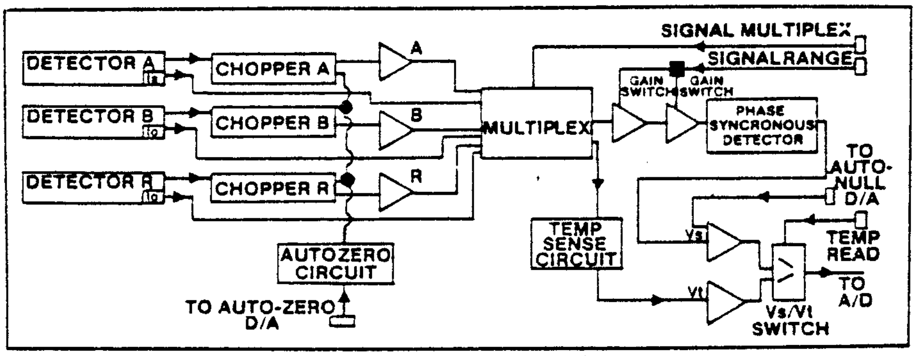


Fig. 3 Input circuitry

25. In order to ensure that the correct gain is selected a status value is read from the A-D converter which is checked to determine whether over or under range. A comparison is made by a digital comparator and the gain shifted up or down until a valid A-D reading is obtained.

26. The signal input circuit (AF03/1) also provides a temperature indication, this voltage (0-10 V), is fed via AC12 to the same A-D converter that provides the conversion for the signal channel. AC12 also provides generation of the chopper drive signal to drive the front f.e.t. choppers. This is derived from the line frequency (≈15.625 kHz) and is synchronous with it, (the line frequency is also synchronous with the microprocessor clock). This ensures that no interference patterns generated from the c.r.t. are picked up and affect the signal processing.

27. Because of this synchronizing it is possible to identify pick-up areas on the chopper cycle and avoid them when re-constitution of the d.c. level occurs. The chopper runs at Line/2 (≈7.8 kHz) also ensuring that pick up affects both halves of the waveform identically.

Analogue-digital system and log conversion

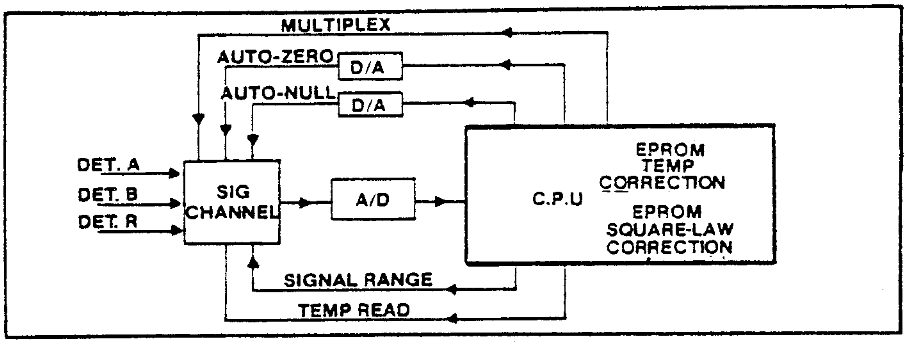


Fig. 4 Data correction circuit

28. The signal channel output (level 0-10 V) is a linear DC analogue of the DC signal provided by the detector and this is fed to the input of the A-D system (AC11). However, the 6511 detector has a "square law" (approximately) relationship between input power and output voltage. To allow for this (to give a linear relationship to the RF level) the signal channel signal is converted to the logarithmic value. The conversion to logarithmic value is accomplished digitally after A-D conversion. Two PROMs contain log data so that the combination of an A-D converter and two log PROMs form a log A-D converter. It is the data from the PROMs that the microprocessor reads. No linear data is available to the microprocessor.

29. Board AC11 also contains the latches which hold the signals controlling the channel multiplexing/gain/temperature select etc., signals which are written in by the microprocessor and then routed to the signal channel (AC12). No digital processing occurs on boards AC12,AF03/1 thus minimizing microprocessor noise effects and ground noise.

Port control

30. The generation of the sweeper ramp, plotter drive signals and the zeroing voltages required by the signal channel is provided by the In-Out interface board (AC09/2). There, D-A converters are formed either by 8-bit latches followed by the D-A, or a 12-bit D-A with the latches integral within the IC. The D-A converters are all controlled exclusively by the microprocessor and are designated as follows :

(1) 8-bit Y-Ramp (plotter)
(2) 8-bit Null voltage
(3) 12-bit X-Ramp (plotter)
and in addition a switch,
(4) Plotter pen lift
(5) 12-bit Auto-zero

Note ...
The plotter output BNC terminals are disconnected when not in the PLOT mode of operation, this is to prevent erroneous operation of the plotter.

Further description of the operation of these ports is given in the paragraphs describing the software concept.

Keyboard and spinwheel

31. The software is structured in such a way that when no control is being exercised over the operation of the instrument, either by the GPIB or the front panel keyboard, the instrument remains sweeping (with a few exceptions). A simplified structure would be as shown in Fig. 5 below.

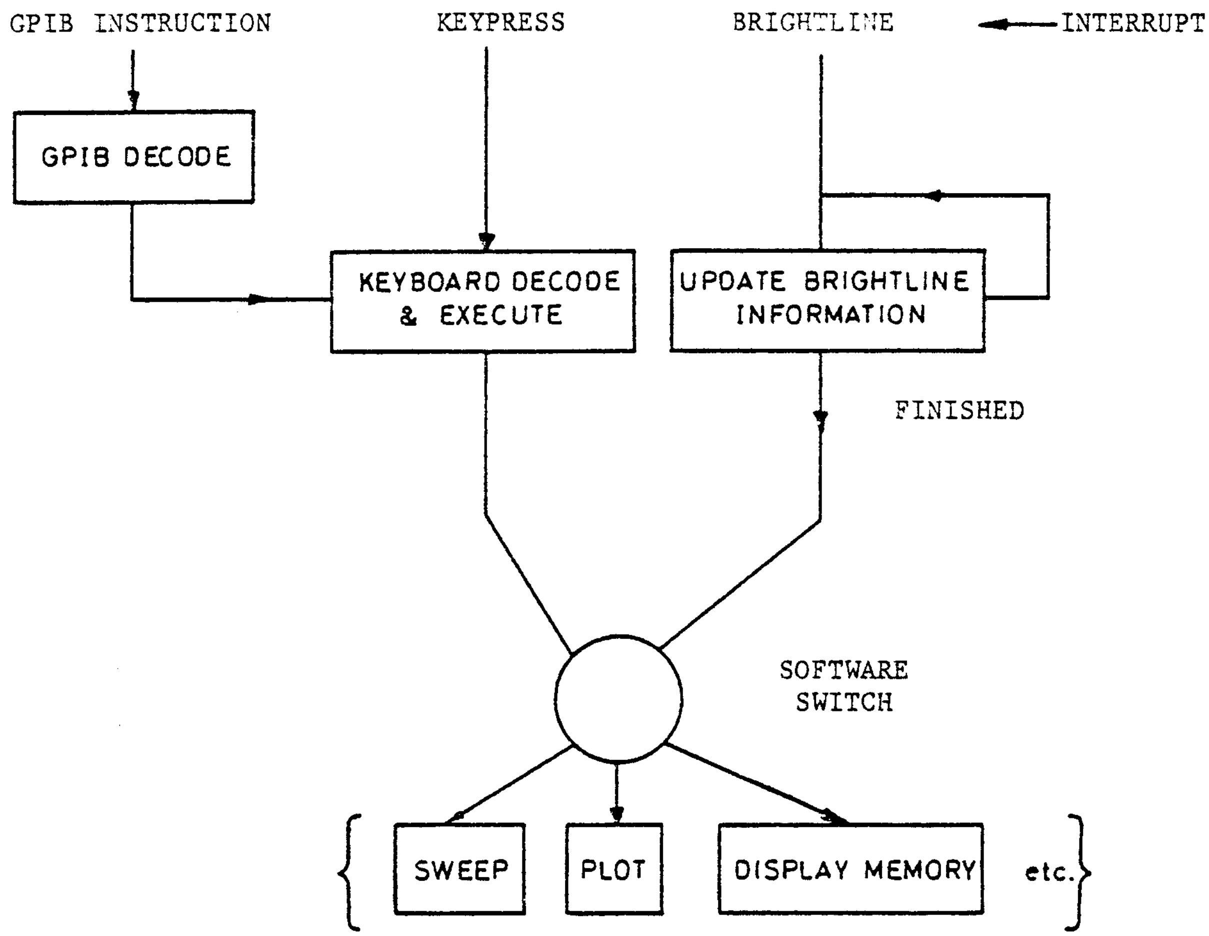


Fig. 5 Simplified software structure

32. Any of the functions; moving the brightline, sending of GPIB information, or pressing a key, will interrupt the current operation of the instrument to re-assess the requirements of the user i.e. a mode change or the changing of a parameter.

33. All the keys are held on board AF01, each key having two (used) contacts normally in the open circuit condition. They are positioned in a matrix of lines such that each key has one 'X' and one 'Y' line connected to it, no two keys having the same pair. A standard KR-2376 keyboard encoder (situated on board AF02) or its equivalent is used to scan the keyboard continually to check for operator intervention. The device will check first to ensure that this is not a spurious response (de-bounce) and then generate a unique code and an interrupt signal to the microprocessor.

34. The Brightline control comprises a motor and operational amplifier window comparator which converts d.c. generated by movement of the motor to a chain of pulses. A direction signal is also derived. The pulses produced generate interrupts to the microprocessor, these and the direction signals are accessed on a port to be read by the microprocessor for control of the Brightline's position and up-date of Brightline information.

35. The pulses are generated by an integrator, and two comparators in parallel, when the comparator 'trips' a pulse is generated setting the direction flip-flop and resetting the integrator.

DETAILED TECHNICAL DESCRIPTION

Power supply unit (AR06)

Circuit diagram : Chap. 7, Fig. 13

36. This is a conventional torroidal type transformer and bridge rectifier configuration with IC regulators, each of which is protected by IN4004 rectifier diodes. The unit is mechanically designed to detach completely from the instrument for ease of maintenance. The cooling fan is mounted within a box used as a heatsink on which the high dissipation regulators are mounted. Each regulator features internal shutdown operating in the event of an overload or if operating temperatures are exceeded. These obviate the need for crowbar or trip circuits.

37. The mains input socket features a mains filter as a standard protection against spurious noise spikes. The mains supply range 120 V or 240 V is set by a slider switch situated on the rear panel, its position being locked by a reversable cover plate indicating the selected range. Primary and secondary tag boards are provided to allow easy disconnection of transformer, fan, mains, input socket and mains switch connections.

38. The torroidal transformer T1 is fixed to the chassis using embedded brass threads in the centre for mechanical strength. The secondary tag board also incorporates secondary fuses F3 to F7, 250 mA-T (250 milliamp time lag) providing overcurrent protection for all supplies except the +5 V and +12 V lines, these are adequately protected by the two input primary fuses F1 and F2.

39. Regulated voltage supplies, regulated +24 V, +15 V, +12 V, +5 V, and -15 V d.c. voltages are used to power the 6500. Additionally, two further independent +15 V and -15 V supplies are provided for the analogue circuits.

40. Two diodes are fitted between chassis and the OVA and OVD terminations. D7 and D8 situated on board AR02 give added protection should the continuity of OVA and OVD be interrupted when the power supply unit is removed for servicing.

41. ±15 V Regulator assembly (AR01), +15 V and -15 V supplies are derived on this board. D1 and D4 form the full wave rectifier bridges, C1 and C4 the reservoir capacitors. Regulators IC1 and IC2 are protected against possible discharge currents in the event of an open circuit by D2, D3, D5 and D6. Fuses FS5 and FS6 give protection to the transformer which otherwise might suffer damage in the event of short circuit. Capacitors C2, C3, C5 and C6 improve the ripple rejection of the regulators and prevent unwanted oscillations.

42. ±15V Regulator assembly (AR02), this assembly operates in an identical manner to the AR01 regulator described above and provides independent +15 V and -15 V supplies to the analogue signal input board AC12 and AF03. D7 and D8 provide protection when board earth terminations are disconnected.

43. +12 V Regulator assembly (AR03), the printed circuit board, IC2 and D2 full wave rectifier, are all mounted on a heat sink. C1 and C7 are the reservoir capacitors, D1 and D2 give protection from accidental short circuits. R1, R2, C2 and C3 improve the ripple rejection. The output also provides a supply to the front panel MAINS ON/OFF l.e.d. the voltage is dropped from +12 V by R1 situated on board AR07.

44. +24 V Regulator assembly (AR05), the assembly p.c.b. is mounted on the heat sink and employs a pre-regulator TR1, R1, D2, C2 dropping the voltage to avoid over power dissipation in IC1 regulator. This supply is made available to the Ramp circuit, board AR04 and is used to generate the 0-20 V variable ramp.

45. +5 V Regulator (AR06), this is a high current regulator which has all its components mounted on the heat sink with the exception of three capacitors C8, C9 and C10, which provide smoothing. All earth terminations are coupled together at one point on the motherboard for best possible ripple rejection and transient response.

Keyboard and spinwheel control (AF01/AF02)

Circuit diagrams : Chap. 7, Figs. 9 and 10.

46. The front panel keyboard assembly is made up of two p.c.b.s, AF01 holds the key switches on a matrix and is coupled to AF02 p.c.b. by Flexistrip cable. AF02 holds all the decoding circuits to present to the microprocessor an interrupt ($\overline{INT}$) and a unique data code for the key pressed. Interrupt pulses are also generated by the spinwheel control circuit. Key and spinwheel data is present on two ports for reference by the microprocessor when running the interrupt routine.

47. All the front panel keys on AF01 are held on a matrix of X and Y digital lines. Each key is connected in such a way that it has its own unique combination. IC1 on board AF02 is a complete keyboard encoder/scanner continually scanning the matrix for a response from the keyboard. When a key is pressed a response is received. Scanning pulses are sent out on the X set of lines and key press replies are received on the Y set of lines.

48. The clock frequency and de-bounce time is determined by R2, C2 and C1, R1. De-bounce time is a finite time that a key press response has to remain active before it is entered as valid data. A properly executed key stroke will produce a strobe output on IC1 pin. 16.

49. The data for the keyboard will appear on IC1 pins 10-15 when the strobe is active. This data is made available to the microprocessor by reading the 'Keyboard data port', IC8, and the strobe data at the 'Spinwheel data port', IC9, via IC2. The strobe is also used to assert the interrupt ($\overline{INT}$) line (via R26 and TR3) on AM01 bus. This is in turn tied to the microprocessor and causes execution of the current program to pause (providing interrupts are enabled) and execute the interrupt handling procedure located at program memory address 0038H.

50. IC2 operates as a 'Strobe enable'. Once this has been latched it remains valid until the microprocessor addresses the latch via IC10 pin 12, at which time the strobe is cleared but not re-enabled.

51. On receipt of a second pulse the latch is re-enabled, this allows the microprocessor to have control over interrupts preventing another key stroke (that could possibly be made during the interrupt handling) from causing incorrect operation. The microprocessor only enables the strobe when it has completed the first key stroke operation.

52. A third port, the 'Front panel l.e.d. drive' is formed by a simple dual flip-flop, IC11. Data determining the on/off state of the two front panel l.e.d.s can be written in at any time by setting up the D0 and D1 data lines on IC11 pins 12 and 2 via SK1 and AM01 motherboard and strobing the clock (with the $\overline{WR}$ line). The two outputs drive TR1, TR2 via R23, R24 with R21, R22 acting as the l.e.d. current limit resistors. The lines are then connected to AF01 l.e.d.s via a flexistrip connector pins B6 and B7 where they complete the earth return for both SHIFT and LOCAL l.e.d.s. The positive terminal of these are wired directly to the +5 V digital supply via pin B5.

53. IC10 provides port decoding for this board, with select pulses being placed on one of the output lines on pins 11-15. The port is only active when either a $\overline{RD}$ or a $\overline{WR}$ instruction is asserted.

54. Brightline (spinwheel) control, IC3 and its associated components form an integrator, nulled by R27. An e.m.f. is produced when the spinwheel motor is turned which is added to the voltage at IC3 pin 6. Providing that the voltage is sufficient (i.e. the motor is turned fast enough) it will reach a potential determined by the 'Window comparator'. This is formed by IC4 and IC5, the higher voltage limit of the window is determined by R8, R9 and the lower voltage limit by R13, R14. When either of these limits are reached either IC4 or IC5 will latch to approximately 0 V, due to the positive feedback employed via R10 and R11.

55. One function of the window comparator is to operate the flip-flop IC6d/IC6e, this is set to indicate the 'Direction', its output is placed on the data bus via IC7e and IC9 pin 4. This data remains valid until the direction of the spinwheel is changed, when this occurs the flip-flop changes state and with it the data output. Details of this and other output conditions are shown in Fig. 6 below.

56. A further output of the window comparator IC4, IC5 is ORed by D2, D3 to give a negative-going short duration pulse which is buffered and stretched by the action of IC6a, C4/R16, IC6b, and IC6c to give a positive output pulse of approximately 1 ms duration. This is used to supply signals for the following :-

(1) A PULSE logical 'low' signal via IC7a and D6.

(2) A DIRECTION signal buffered onto bit 7 of the data bus via IC7c/IC7d and IC9 pins 2/12.

(3) Integrator reset, the 1 ms pulse is fed via D1 to the gate of TR4. This f.e.t., normally turned off, is switched on by this pulse as the window voltage limit is reached. The pinch off voltage of the f.e.t. is critical and care is taken to ensure that as IC3 voltage rises the bias does not turn TR4 on before reaching the window comparator limit. IC3, integrator resets as TR4 turns on and almost instantaneously TR4 turns off, until once again the voltage output of IC3 pin 6 reaches the window limit voltage and the cycle is repeated.

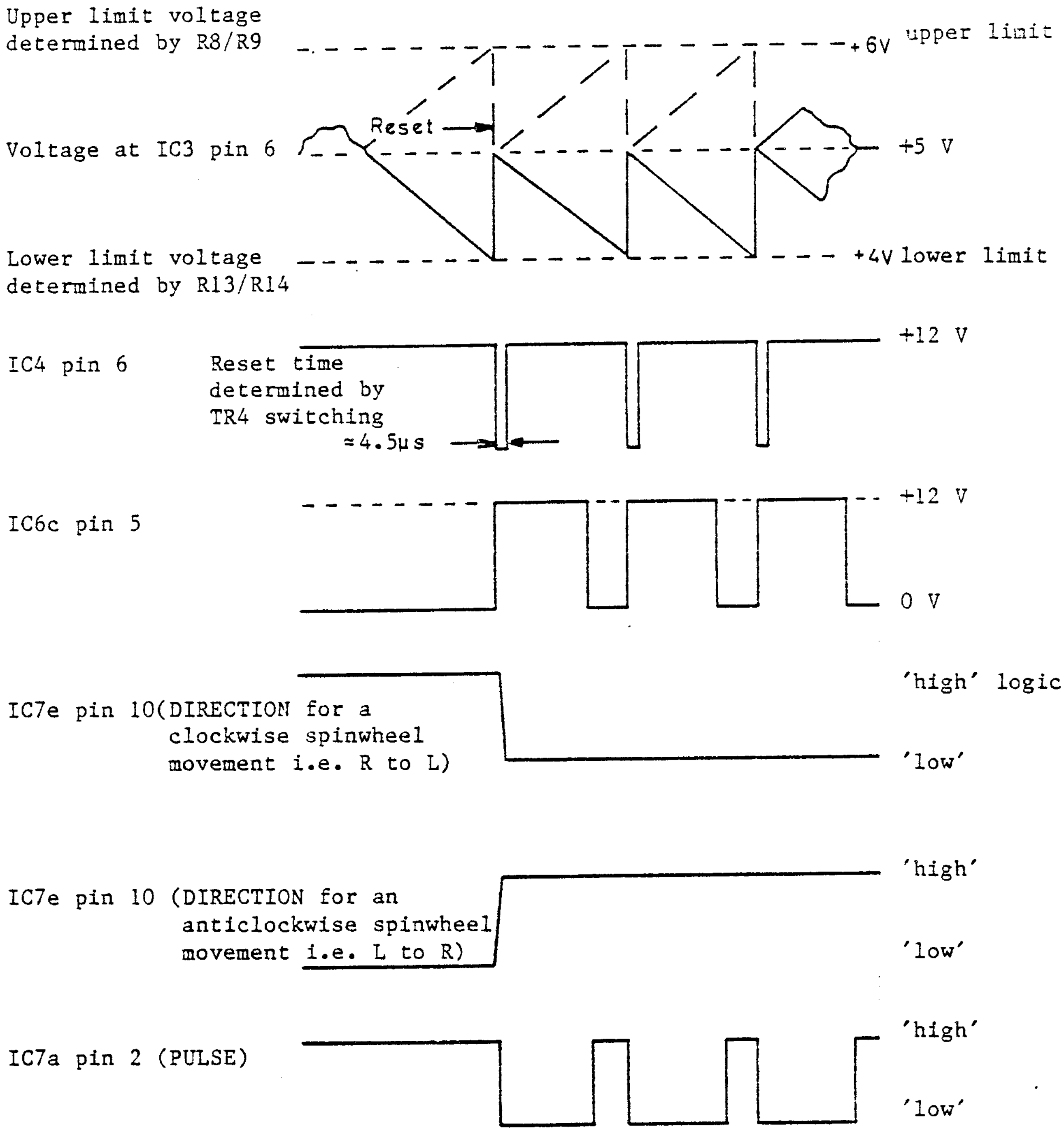


Fig. 6 Spinwheel (Brightline) control timing waveforms (AF01/AF02)

CRT (AT01/1 & AT02) ⚠

57. When exposing the c.r.t. care must be taken to prevent implosion and possible scattering of glass fragments. The c.r.t. employs high voltages (+12 kV) which are capable of internal flash-over or tracking from the anode cap or any other high voltage area. It is therefore important to ensure that if this were to happen the current would be conducted safely to earth. To achieve this a base sparkguard has been fitted, this board supports the c.r.t. base socket and is made from fire retardant material to prevent scorching, and has spark gaps punched into it. These protect the semiconductors on AT01/1 in the event of a high voltage flashover.

58. Line drive. The line drive is synchronized to the positive-going t.t.l. line sync pulses appearing at PL1 pin 5. These pulses are inverted and level shifted by TR4 to provide trigger pulses for IC2 which is a timer IC connected for monostable operation. The output pulse width of IC2 is adjustable by R31. This alters the phase of the final drive relative to the incoming sync pulses and provides control over the vertical position of the displayed information within the raster area. IC3 is a second timer device which is connected for astable operation at approximately line frequency (15.625 kHz), but is synchronized by re-triggering from the output of IC2 via D3. The astable mode of operation is chosen so that removal of the incoming line sync pulses will not result in the loss of drive to the line output transformer, T1.

59. The output of IC3 is buffered by TR5 and drives TR6 via C23 which improves the turn-off characteristic and R37 which limits the base current. TR6 drives the line deflection coils in parallel with the primary of T1. During the period when TR6 is turned on the energy stored in C30 is discharged into the yoke causing the c.r.t. beam to scan vertically across the screen. When TR6 is turned off the energy stored in T1 is transferred to C24 which discharges into the yoke causing the c.r.t. beam to be rapidly deflected back to the bottom of the screen. L1 regulates the current flow through the yoke and provides a line amplitude control. In a similar manner L2 provides control over line linearity.

60. Secondary voltage supplies. The secondary windings of T1 provide four secondary voltage supplies required by the circuit. The final anode voltage of +12 kV is generated by an overwinding on the transformer which has an integral rectifier moulded into the assembly. The output is taken directly to the c.r.t. via the red e.h.t. lead and anode cap.

61. D8 and C27 provide rectification and smoothing for -50 V which is used as a negative supply for the brilliance control. TR7 is normally turned on but on power down the base voltage collapses causing TR7 to switch off. The c.r.t. grid voltage rises, flooding the tube and extinguishing the display.

62. D10 and C26 provide +100 V which is used as a positive supply for the brilliance control and also the video amplifier.

63. D9, R39 and C28 provide +480 V which is required for the focus control and also provides the A1 voltage via a potential divider R42 and R43. The A1 voltage is further smoothed by C29.

64. Frame drive. The frame drive is based on IC1, a TDA 1170S, and is a standard application circuit for this device. The oscillator free-run frequency is determined by R1, R48 and C4, which provide a frame lock control. The oscillator is synchronized to the incoming frame sync pulses on PL1 pin 6,

which are applied to pin 8 of IC1. R2 and R3 control the amplitude of the internally generated ramp and hence the width of the display. The network around R6 alters the shape of the ramp, providing a frame linearity control. The characteristics of the output stage of IC1 are set by R7-12 and C7, C9 and R13 damp the high-frequency transients generated during flyback. C10 acts as a d.c. current block.

65. Video drive. The video signal is input on PL1 pin 4. TR1 acts as an emitter follower supplying the video driver TR3 which provides current amplification. The response of the circuit is set by R21 and C14. TR2 is a voltage amplifier whose d.c. operating point is set by R17. R17 is normally adjusted for +70 d.c. at the collector of TR2. The video drive output is fed directly to the cathode of the c.r.t.

66. Flash-over protection. When a flash-over occurs within the c.r.t the final anode capacitance is rapidly discharged through one of the c.r.t. electrodes. The resultant voltage spikes are prevented from damaging the circuitry by a resistor and a spark-gap at each electrode junction. The resistor presents a high impedance path to the spike, whilst a low impedance path is presented by the spark-gap when ionized. Thus the discharge current is routed back to the external c.r.t. coating, preventing large currents from flowing through the c.r.t. circuitry.

Timing circuit (AC01)

Circuit diagram : Chap. 7, Fig. 1

67. All data required to form the timing signals to provide the various display layers are held in permanent memory using a control PROM. One PROM holds signal data occurring at line rate, another holds the Frame orientated signals. Counters address the PROMs and the contents are latched out to prevent spurious signals. This method ensures that no phase delays result, these could otherwise cause jitter or blurred detail.

68. The display is interlaced (alternate frames formed by scanning the beam across the screen, bottom to top, left to right, are offset by half a vertical line width), see Fig. 8 for details. This standard TV method allows higher resolution on the c.r.t. AC01 controls and synchronizes signals on other boards such as AC02,3,4 and 5, no actual video signals are present on AC01.

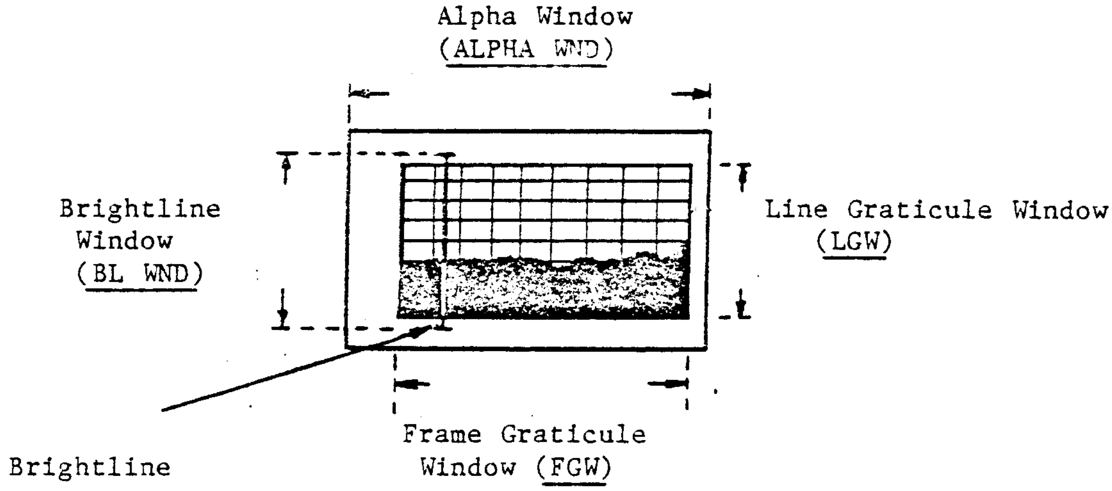
69. Line orientated signals, the fundamental 5 MHz clock frequency from the microprocessor AC18, (Lx320), is fed to buffer IC1d via pin A32 to give a noise free clean edged clock pulse. IC2 pre-scales IC1d clock output and IC3 synchronizes the signals to the 5 MHz clock. IC3/Q2 output provides a latching edge to latch into IC7 the line timing data from IC6.

70. IC4/QA output provides a line x2 clock for board AC12 chopper circuit with the remaining outputs of IC4 and IC5 combining to form a 6-bit counter which is used to address IC6 'Line timing' producing a line ≈ 64 µs digitized to 64 steps. The counters IC4/IC5, are reset at the end of each frame to ensure synchronization.

71. Each output of IC6 forms a digital signal repeated at line rate, the data for these are given in the Software archive. The following lines are constituted:-

Q0, Lx32S (A21)	Synchronized 'LINE x 32S'freq. used to enable the alphanumerics (ALPHA) shift register on the Alpha Generator board AC05.
Q2, $\overline{\text{BOL}}$ (A9)	'BEGINNING OF LINE' cycle (pulse active low) used to load line position on Line Generators A & B boards AC02/AC03. Also used on Character column address ÷6 circuit AC05.
Q3, $\overline{\text{LD ARAC}}$ (A6)	'LOAD ALPHA RAM ADDRESS COUNTERS', loads Alpha address timing counters on board AC05.
Q4, LGW (A3)	'LINE GRATICULE WINDOW' used as a gating pulse to determine the graticule window on boards AC02/AC03/AC04/1. That is the portion of a vertical scanned line forming part of the displayed graticule.

Q5, HORIZ.GRAT (A20)	'HORIZONTAL GRATICULE' enables the 11 horizontal graticule lines on the Video circuit board AC04/1.
Q7, BL WND (A13)	'BRIGHTLINE WINDOW' gating pulse used on board AC04/1. (Vertical portion of scanned line over which the brightline is generated).
Q2, LINE DRIVE (A19)	This pulse is derived from the $\overline{\text{BOL}}$ line and is inverted and buffered by IC17e and fed to the c.r.t. SK1 pin 5 as a sync pulse (LINE SYNC) for locking the c.r.t. drive to the line frequency.
Q1, $\overline{\text{LINE BL}}$	'LINE BLANK', IC7, Q1 is asserted 'high' before the LGW instruction to ensure that the oscillator formed by IC1a & b, R10, R11, C12 is oscillating before the Line counters AC02/AC03 are gated ready by the LGW signal. The synchronizing is necessary as the oscillator is asynchronous and would otherwise clock AC02/AC03 at a time varying by one cycle. This would show as a jittery line display on AC02/AC03 LINE VIDEO output. The oscillator must be adjusted by R11 such that 256 cycles occur during each LGW at line period.



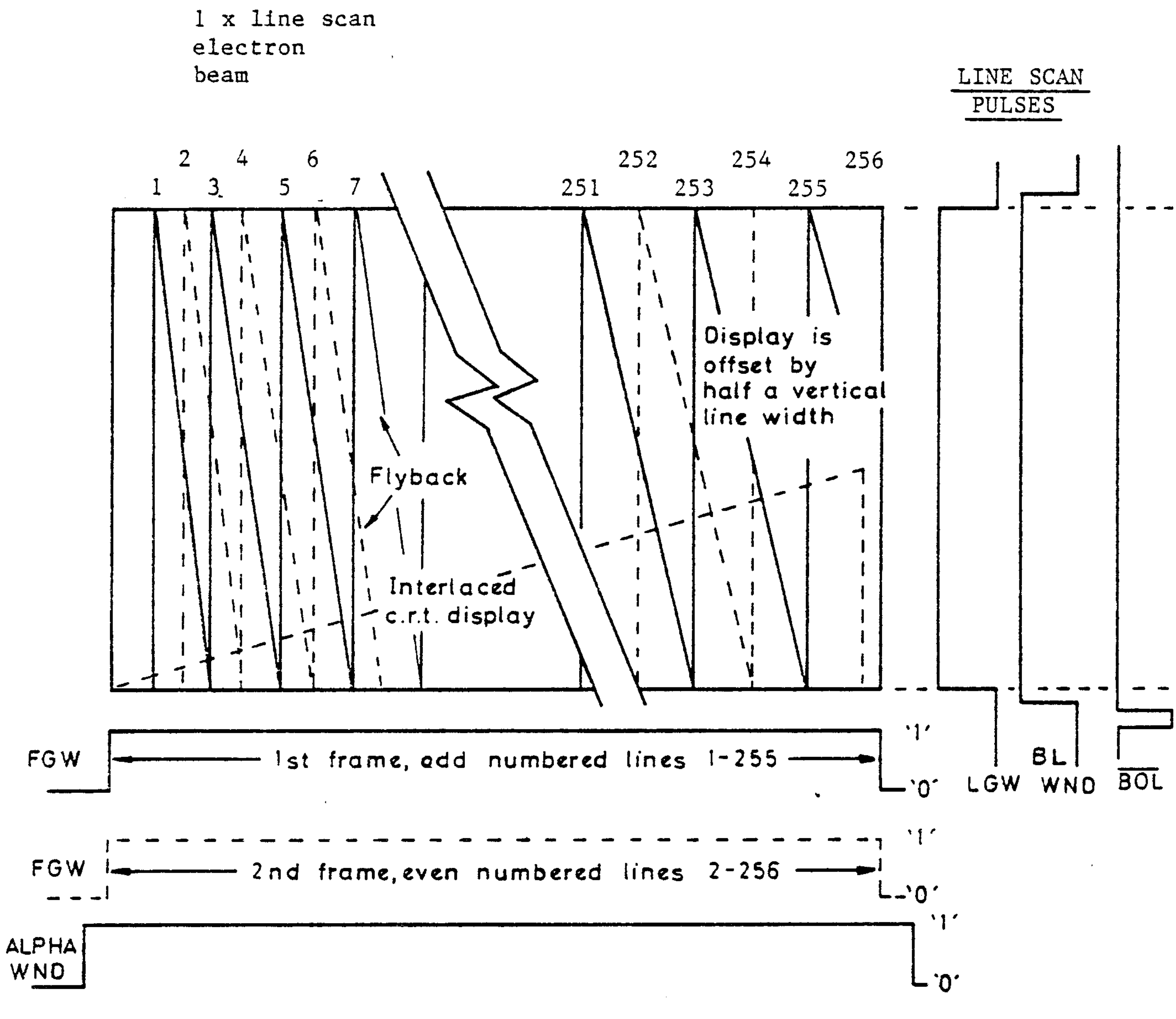


Fig. 7 Interlaced c.r.t. display (AC01)

72. **Frame orientated signals**, these are derived in a similar manner to the line signals, the address to IC9 'Frame timing data' is counted by IC8, clocked at line x 2 in order to achieve the required interlaced display. The least significant bit is not used to address IC9 2 K byte EPROM, one count is missed every frame scan by gating IC16a with a pulse longer than line ÷2 from IC5 pin 11 and a shorter than line length pulse generated at IC11 pin 7.

73. IC8 pin 12 (Q9) output triggers the monostable flip-flop IC11 to provide a frame sync pulse 'FIELD DRIVE' buffered by IC16d and fed to the c.r.t. AT01/1 board. IC10, 'Frame timing latch', provides the frame signal's latch data asserted at the beginning of line blanking. A combination of line and frame pulses are gated by the following :-

Q0, IC13a CK ARAC (A5)	'CLOCK ALPHA RAM ADDRESS COUNTERS' only occurs during 'ALPHA WINDOW'.
IC13b VIDEO BLNK (A7)	'VIDEO BLANKING' (composite) line and frame blanking.
IC13d/IC16c/IC17d LINE GEN CK (A1)	'LINE GENERATOR CLOCK' used on boards AC02/AC03

74. Latched outputs from IC10 that are exclusively frame pulses are constituted as follows :-

Q0, ALPHA WND	'ALPHA WINDOW' Alphanumeric information is enabled during this period.
Q1, $\overline{\text{FR BLANK}}$	'FRAME BLANKING'
Q2, FGW	'FRAME GRATICULE WINDOW'
Q3, $\overline{\text{END 1st FR}}$	'END FIRST FRAME' Logic low level indicates that the first of the two scans is completed - required in generating the line displays.
Q4, $\overline{\text{RESET ARAC}}$	'RESET ALPHA RAM ADDRESS COUNTERS' A logic low level resets the RAM address counters at the beginning of a scan.
Q5, VERT GRAT	'VERTICAL GRATICULE' This signal is no longer used.
Q6, $\overline{\text{PR ARAC}}$	'PRESET ALPHA RAM ADDRESS COUNTERS' Presets the RAM address counters with data on board AC05 pin A10.

75. IC9 holds different data for the two frames (512 data bytes) and is addressed in such a way that the frame data is entered sequentially through from line 1 to 512 and is not interlaced for each frame. This simplifies the programming of the EPROM. IC8, Q0 addresses IC9, EPROM. IC16b, IC17c, D1, R2 and C1 form a pulse to reset the line counters after every complete set of two scans. Resistor R1 allows conversion from TTL to CMOS levels. S1 allows unused areas of the EPROM to be used for test purposes, at present this data is not utilized.

Line generators A and B (AC02/AC03)

Circuit diagram : Chap. 7, Fig. 2

76. The AC02 and AC03 boards are identical apart from two wire links which select either LINE A or LINE B to set its position in the memory map of the microprocessor. The board's function is to provide a CRT display of measurement results in line or histogram format. AC02 (LINE A) provides a display of traces for CHANNEL A or CHANNEL R, and AC03 provides the display for CHANNEL B.

77. IC9 and IC10, Line display memories hold the display data in consecutive locations i.e. Display values 0 to 421 (from left to right) are stored in the RAM addresses 0 to 421. The height of a vertical line trace component is dependent on the data (0-255) stored at the corresponding RAM location. Data 0 corresponds to the top and data 255 to the bottom of the trace respectively, as shown in Fig. 8.

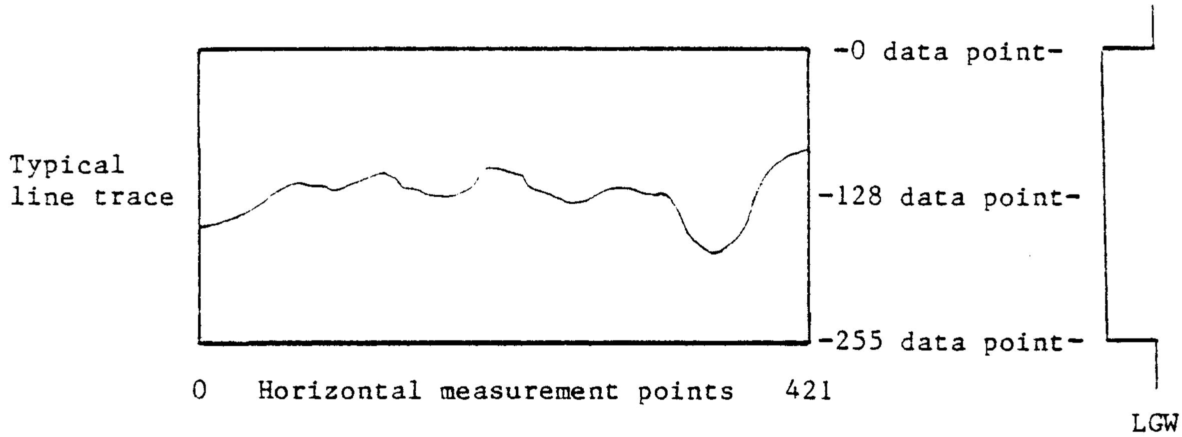


Fig. 8 Display data location (AC02/AC03)

The memory is accessed by both the microprocessor and the display circuits. Output from the line generator is in the form of a simple t.t.l. video signal.

78. IC1 and IC2 carry out the decoding of the microprocessor address for the board. IC4 buffers data input/output from the RAM IC9, IC10 and the microprocessor and also isolates the board from the data bus when it is not being updated. When the microprocessor is not addressing the RAM the display circuitry accesses it as addressed by the counter IC8 counting at line frequency (15.625 kHz), IC3, IC6, IC7 data selector/multiplexers switch the address information to the microprocessor bus when it demands the memory and reverts back to the display mode on release; Microprocessor access causes IC2, pin 15 (AC02) or pin 13 (AC03) to be asserted 'low' switching to the microprocessor bus. The second output from IC2 on pin 14 (AC02) or pin 12 (AC03) is used as a port; address bit D0 is latched into IC18 to control the selection of either LINE or HISTOGRAM display.

79. **Histogram display.** Considering this selection first, as IC8 output address progresses from 0 to 421, data can be loaded into IC13, IC14, IC15 and IC16 and the data up counted. During the LGW period the up counting is carried out by the 'LINE DOT CLOCK' (256 cycles for each LGW instruction) with a 'Carry out' occurring at a time determined by the data. Data of 255 will appear immediately at the bottom of the screen, data of 128 in the centre, and 0 at the top of the screen. Histogram display is in fact a modification of the Line display which is more difficult to achieve.

80. **Line display.** When HISTOGRAM is selected bright up occurs from the bottom of the graticule, up to the data point for each line. To provide a LINE display a line must be drawn from one data point to the adjacent point on the next line; consider the display shown below.

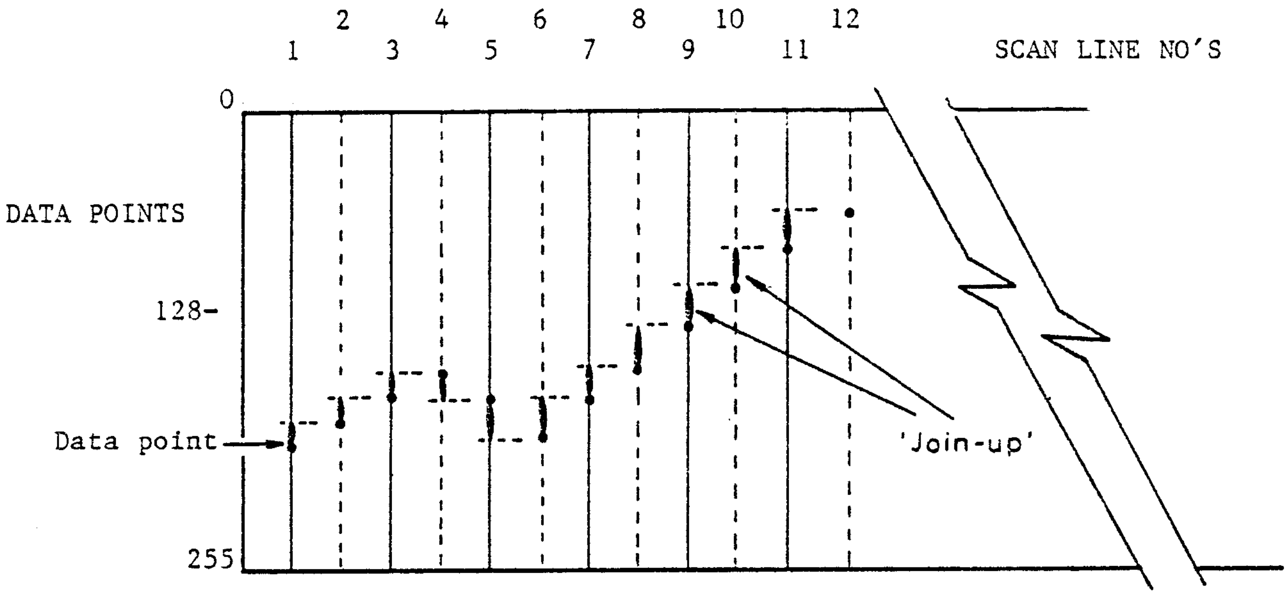


Fig. 9 Line display data/join up points (AC02/AC03)

81. The dots represent the data in memory, scan lines 1,3,5,7 etc. occurring on the first frame and 2,4,6,8 etc. on the second frame. Joining up from one data point to the data point on the line following is accomplished by accessing the data corresponding to both frames. Data is loaded into counter pairs IC13/IC14 and IC15/IC16 from the RAM IC9 and IC10.

82. The instruction $\overline{BOL}$ acts as a steering pulse to load one of the counter pairs. When this is asserted 'low' IC13/IC14 can be loaded. Two pulses are generated on the LINE GEN CK line, the first of these is steered to one of the counter pins via IC4 and IC17a-c. In between these two LINE GEN CK pulses IC8 is clocked to provide the next address therefore causing two loads to occur during each line.

83. On the second frame after IC8 counter has been reset one pulse is generated to offset the line count by one to provide the interlaced frame line connections (2-3, 4-5 etc.). When loaded, both sets of counters start to count up until the first 'Carry-out' occurs, this clocks one of IC19's flip-flops, changing the state of IC20c to output the line video signal (A4,A5). IC19's other flip-flop changes state when the second pulse,

corresponding to the higher data loaded, falls out of 'Carry-out' to restore IC20c to its original state and therefore ends the line video signal output at A4,A5.

84. The initial condition of IC19 flip-flops are set by the LGW to hold both outputs 'low'. Both are connected in a divide by two configuration, if the data points on two adjacent lines are identical neither flip-flop would change state and therefore no video output would result. C4 C5 R7, R8,D1,D2 and IC22c therefore provides detection of coincident pulses and a horizontal line of a duration determined by C6,R9, is produced instead by IC21, further gating of the video is carried out by IC22a,b, to prevent operation of line display outside the frame graticule window.

85. <u>LINE/HISTOGRAM selector (IC18)</u>, the selector acts as a write-port from the microprocessor. A selection of HISTOGRAM sets a 'low' output at pin 5 which in turn disables the second flip-flop IC19(Q2) by holding down its 'clear' input. Hence at the start of the LGW signal video continues to be output until turned off by the current lines 'Carry-out'.

86. <u>Microprocessor access de-glitch circuit</u>, IC5 provides the pulses for counter loading. If microprocessor access occurs at any time during these pulses, a secondary load pulse is generated to replace the one made ineffective by the microprocessor access, otherwise incorrect data could be loaded to the counters. The secondary load pulse occurs by detecting the switch-over of the data selectors and generating a pulse covering the time during which data is invalid - a $\overline{RD}$ or $\overline{WR}$ takes approximately 0.5 µs and IC6 and IC7 data multiplexer outputs will settle within 1.5 µs. When a counter load pulse (IC5, Q1, pin 13) is detected coincident with a microprocessor access IC5's second monostable input (pin 9) triggers via IC1c to provide a replacement pulse some 2 µs later on its output (pin 12). Both of IC5's outputs are gated together in IC17a. The above circuit improves the glitch free operation significantly although if microprocessor and line (15.625 Hz) frequency are not locked other timing problems would be likely to occur.

Note ...

> The board's line display memory is not accessed by the microprocessor when in FREEZE mode of operation, and fastest access occurs when speed 0 (70 ms) is selected, useful for test purposes.

Video circuit (graticule) (AC04 /1)

Circuit diagram : Chap. 7, Fig. 3

87. Video mixing for boards AC02/AC03, AC04/1, AC05 video signals occurs on AC04/1. In addition video signals for the graticule lines and Brightline markers are generated. A read-port is also provided to enable the microprocessor to sample certain timing signals during self-test and normal operation. Each video signal is gated with an enable to allow portions of the display to be switched off. Markers and Graticule lines are held in memory, the position across the screen corresponding to the address. The data (a four bit word) for each scan line is arranged such that one bit corresponds to one signal, therefore allowing for four different vertical lines to be generated if required. The method for addressing the RAM is identical to that used on board AC02/AC03 i.e. switched between microprocessor and timing signals.

88. The data for graticule etc. line placement is held in the 1Kx4 RAM, IC8 and the address to it generated by the counter IC5 or the microprocessor address bus. Switching from one to the other is carried out by IC6 and IC10 data selectors when the block decode is detected by IC3 pin 9 which decodes IC8, memory block 5COOH. IC7 is the data bus buffer for IC8.

89. IC2 and IC4 provide decoding and allow data to be read from IC1 'Timing signal port' and written to IC12 'Display enable latch'. Various timing signals are provided on IC1 for self test purposes; to ensure correct timing signals, and provide blanking on access to the Alpha memory (the Alpha memory is only accessed by the microprocessor during line blanking periods).

90. The microprocessor can also write to IC12, Display enable latch to control which aspects of the video can be gated through to the video mixer. IC9 monostable generates ten narrow fixed horizontal graticule lines, these are triggered by transitions of the HORIZ GRAT signals (B20) originating on AC01 Timing board. The remainder of IC9 could be used to generate small tick markers coincident with the start of the LGW although these are not now used, they can be generated merely by setting the appropriate bit in IC8 RAM location.

91. Gating is carried out by IC11a,b. Assuming no microprocessor interference, data is clocked out of IC8 every scan line by clocking IC5 counter at line frequency using the BL WND (brightline window) signal. Each output bit from IC8 is routed via appropriate gating with the 'window' and enable signals to the 'Video mixer' as follows :-

Line A and B via IC13.

Marker, Brightline and Vertical graticule via IC11 and IC14

Alpha video via IC15b.

The relative brightness of the video signals is pre-set by R11-R16 and final buffering is provided by TR1,TR2 and associated components. Video blanking is applied by TR3, driven by an inverted VIDEO BLNK signal from A7 via IC15c. The video output is taken from pin B17 to the c.r.t., AT01/1 board, SK1 pin 4.

92. The software limits access to IC8 to blanking periods only otherwise video glitches would occur where incorrect data is available during the LGW period. The display enable latch IC12 is accessed whenever either A,B, or R channel is selected to switch on the appropriate line displays.

Alpha generator (AC05)

Circuit diagram : Chap. 7, Fig. 4

93. The function of the Alpha generator board is to provide memory mapped alphanumerics to the c.r.t. as a 41 columns by 25 rows display giving 1025 character locations. Each character comprises a matrix of 8x6 illuminated picture elements or (pixels), vertically spaced by 2 elements. The memory is configured such that addresses increase by 1 from bottom to top and by 25 from left to right across the tube face.

ALPHANUMERICS MEMORY MAP

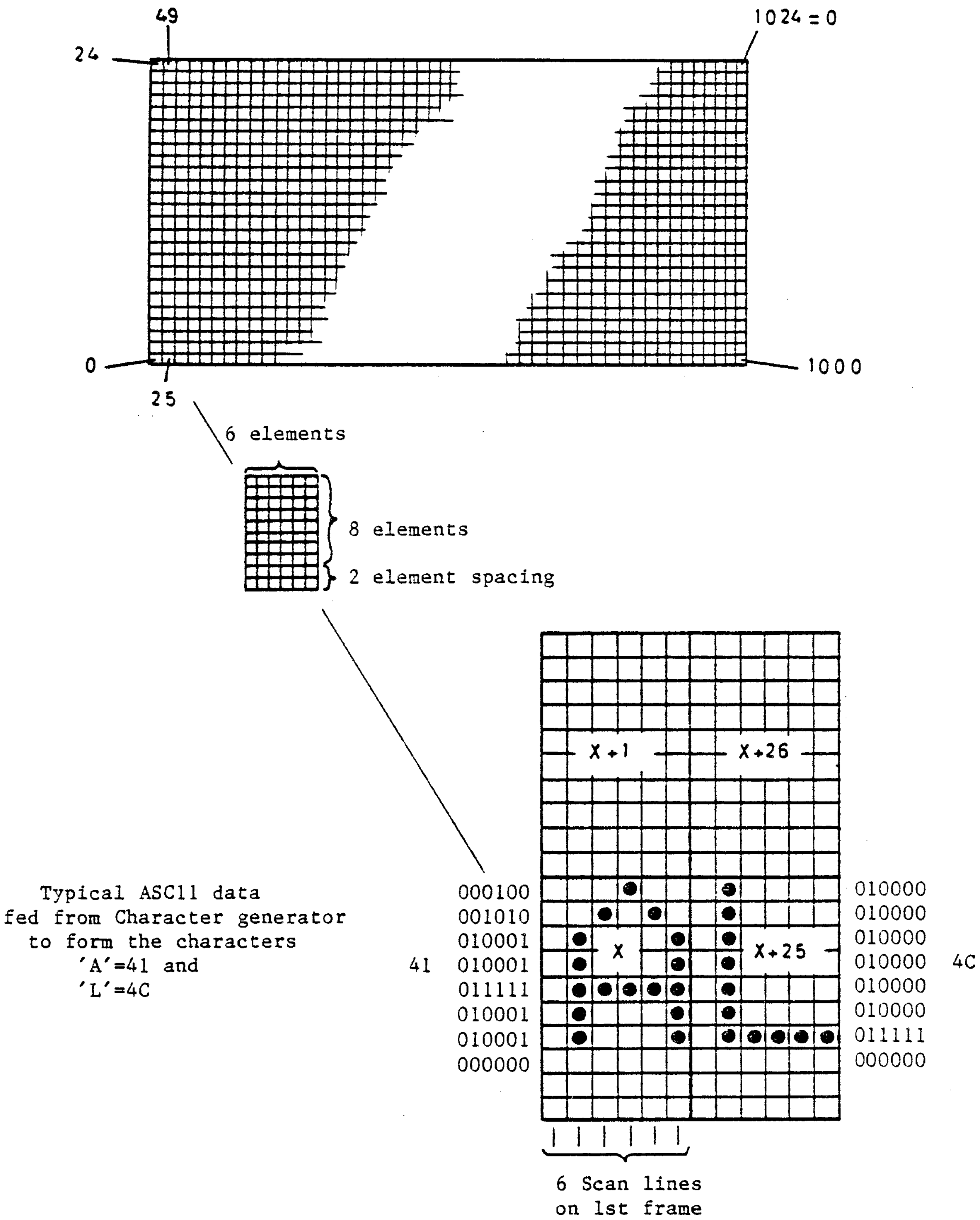


Fig. 10 Alphanumerics memory mapping (AC05)

94. The alpha memory block has 1024 locations, although 1025 locations are mapped (this will cause any character written to the base address to also appear on the top right hand corner of the display). In this board, as with AC02/AC03, and AC04/1, the memory is switched between two sets of address lines - microprocessor, and timing signals. The timing address requirements for this board are different in that each of the locations (e.g. 0-24) must be addressed for six consecutive scan lines followed by a further six for the following 25 locations and so on for all of the 41 columns. This is achieved by a divide by six circuit.

95. For the purpose of the display there is no difference between first and second frame (interlace) so a character block will in fact actually occupy twelve interlaced scan lines. The memory contains data (0-255) which in turn is used to address a character generator which holds the actual picture elements required to make up the character on the screen. The standard ASCII coding is used to generate the characters, and bit 7 (MSB) is used to 'Flash' the character to give extra emphasis to Error messages etc. on the display trace. IC21a,b, provides the gating and conversion in polarity for the alpha bright up video signal output at pin A6.

96. The alphanumeric memory (1Kx8) comprises IC6, IC7. This may be written to as though part of the microprocessor memory map, but is not read back to the microprocessor. Switching between microprocessor and Timing display addresses is carried out by IC8, IC9 and IC10 with each pin 1 asserted logical 'low' to select the microprocessor address. The memory block is decoded at 5800H for 1 K by IC1, the data bus buffer IC4 being enabled by IC5c,d; gating together the enable and $\overline{MEMW}$ signals.

97. The timing address is generated by the divide by six circuit comprising IC2/IC3, this is triggered at line rate by the BOL signal at pin A9. The outputs of the divide by six circuit are used to address the three least significant bits on IC17 Character generator, data being arranged such that adjacent rows (left to right) of the pixel data for each character is held in adjacent, ascending locations of IC17 memory.

98. Data from IC6/IC7 RAM provides the remainder of the Character generator's address to read out of 25 consecutive locations during each line scan as shown previously in Fig. 10. IC17 Character generator data output is then loaded into IC18 parallel in, serial out register at the beginning of a picture element and shifted out by LINEx320 (A32) (LINE being 15.625 kHz). When the next RAM location is addressed at LINEx32S (B21) (S indicates synchronized) 10 pixel outputs will be generated for each pixel vertical line, the last two elements are used as spacing blanks and are kept at logical 'low' level. The serial output of IC18 is finally gated at IC21a with the 'Character flash' circuit IC22/IC23, this is invoked when the data bit 7 is asserted high and gates the output at a rate of approximately 2 Hz.

99. IC21b converts the polarity of the signal to give a 'bright' alpha video output at pin A6. IC20 provides a pulse approximately 100 ns generated by a synchronized version of the LINEx32 signal, this is necessary to prevent any shift in position of the alpha characters which would otherwise cause blurring on the display. IC20 also provides blanking during the time that the video RAM is accessed. This function is largely unnecessary now because the RAM is only accessed during the line blanking period anyway.

100. The RAM address is generated by IC11-IC16. The latches IC14, IC15, IC16 load the contents of the counters IC11, IC12, IC13 when instructed by IC5a pin 1. Gating of the $\overline{\text{PR}}$ $\overline{\text{ARAC}}$ and the $\overline{\text{BOL}}$ signals together at IC5a generate a pulse to enable the COUNTER latches every six scan lines. At the start of a scan line the counters are loaded with the contents of the latches by the $\overline{\text{LD ARAC}}$ signal at pin A3, this follows the $\overline{\text{BOL}}$ signal. The counters are then clocked 25 times by the CK ARAC signal at pin A2 to give a total output from IC11-IC16 of 25 consecutive upward counts which are repeated for six scan lines to form a column of characters. The latches are then loaded with the address of the next column (This is the highest count reached by the counters during a line scan). The $\overline{\text{PR}}$ $\overline{\text{ARAC}}$ signal performs this function and repeats it for the next consecutive count of 25 and so on e.g. Count 0-24; 0-24; 0-24; 0-24; 0-24; 0-24; 25-49; 25-49; etc. The output then being combined to provide the address for IC6/IC7, alphanumerics character RAM.

Microprocessor (AC18)

Circuit diagram : Chap. 7. Fig. 5

101. The microprocessor board contains an 8085A-2 CPU, an internal clock generator operating at a frequency of 10 MHz, 8 K RAM, up to 32 K EPROM (depending on the selection of links 1-4), and buffers for the address and data bus lines. The clock frequency is divided internally to give a 5 MHz operating frequency. Components and the interconnections on this board are briefly described below, a full description can be found in "MCS 85 Users Manual" published by Intel Corporation.

102. The purpose of IC1, CPU is to control the instrument by means of the address and data buses. It is an 8-bit NMOS microprocessor with interrupts, and features a multiplexed address/data bus. It is compatible with software in the 8080 series, but has two extra instructions available and operates faster.

103. R2, C1 provides power for RESET IN, D1 allows C1 to discharge when power is switched off. Three interrupt lines are brought via the edge connector to IC1. GPIB INT (B8) asserts RST 6.5 line high. $\overline{\text{INT}}$ (A19) is an active low bus signal inverted by IC2a and fed to RST 5.5, this is used for spinwheel and keyboard interrupts. $\overline{\text{TRAP}}$ (B4) is another active low bus signal not used at present but made available for future expansion.

104. Address and Data buses are multiplexed, pins A8 - A15 are output-only lines carrying the high-order byte of memory addresses. AD0 - AD7 are bi-directional lines which output the low-order byte of memory addresses and also double as a bi-directional data bus. IC15 latches the low order address lines A0 - A7 on receipt of the ALE (Address Latch Enable) pulse from IC1. IC14 buffers the high order address lines A8 - A15.

105. IC11 bi-directional data bus transceiver direction is controlled by the microprocessor's RD line. IC16 buffers the following miscellaneous control signals; $\overline{\text{WR}}$, $\overline{\text{RD}}$, CLK, $\overline{\text{PRT}}$, $\overline{\text{RAM}}$, $\overline{\text{RAM-UNS}}$. The 5 MHz clock IC1, pin 37 is inverted by IC2f to eliminate display jitter due to noise spikes present on the negative half cycles. The CLK signal is also fed in parallel through IC16 to give extra drive, R6 prevents display jitter by damping any excessive ringing.

106. Address lines A14, A15, are used to decode four 16 K address blocks via IC3a, 0000H - 3FFF, 4000H - 7FFFH, 8000H - BFFFH and C000H - FFFFH. Block 8000H - BFFFH is further decoded by IC3b via address lines A12 and A13 to give the memory mapped port block 8000H - 8FFFH. The 8K x 8 bytes of RAM (read/write) provides the work space and instrument storage for the 6500 and is addressed contiguously. IC5 decodes the four RAM select lines for IC17, 18,19,20, mapping the 8K RAM into the upper half of the 16 K block specified by the $\overline{\text{RAM}}$ signal.

107. Memory locations are accessed when the RAM signal is asserted 'low' to enable IC5, the high order address lines A13,A12,A11, determine the decode output ($\overline{\text{RAM0}}$ - $\overline{\text{RAM3}}$) which in turn enables one of the 2K x 8 RAM memories IC17 - IC20 asserting a CS logical 'low' signal to pin 18. Eight data lines D0 - D7 and eleven low order address lines A0 - A10 are connected in parallel to the memory bank IC17 - IC20. IC11 is an octal bus transceiver and forms a bi-directional buffer to allow data to be either written to the RAM (when IC11 pin 1 is 'high') or read from the RAM (when the $\overline{\text{RD}}$ signal is asserted 'low').

108. IC3,5,6 provide address bus decoding for the RAM, EPROM, INPUT/OUTPUT port address blocks and are defined as follows :-

Block Select Signal	Description	Circuit reference
$\overline{\text{ROM 0}}$		IC7
$\overline{\text{ROM 1}}$	8 K EPROM $\overline{\text{CS}}$	IC8
$\overline{\text{ROM 2}}$		IC9
$\overline{\text{ROM 3}}$		IC10
$\overline{\text{RAM UNS}}$	16 K unsynchronized	Not used at present
$\overline{\text{RAM}}$	Delayed version $\overline{\text{RAM UNS}}$ defines 16 K block at 4000H or C000H depending on link selection	IC12
$\overline{\text{PRT}}$	Memory mapped PORT block select	IC4b
READY (WAIT ON $\overline{\text{PRT}}$ GENERATOR)	Generates a wait state of clock period (200 ns)	IC13

109. Link 1 allows the RAM block to be selected to normal (NRM) operation location (4000H - 7FFFH), or an expanded (EXP) operation (C000H - FFFF) as shown in Fig. 13. As each IC is accessed individually the low order address lines A0 - A10 complete the address to specify which of the 2048 locations are to be read out or written in to. The selected signal is passed directly to IC16 pin 11 ($\overline{\text{RAM UNS}}$) and also to the RAM synchronizer, IC12 where the signal is delayed by half of one clock period. This ensures that the address is stable before $\overline{\text{RAM}}$ is asserted low.

110. **RAM synchronizer IC12.** Spurious addresses can occur momentarily as the above address lines change state. These could cause spasmodic operation of the $\overline{\text{RAM}}$ signal and as a result undesirable switching of the address multiplexers on boards AC02/3 and AC05. This would also result in unwanted glitches in the display. To prevent this from occurring the start of the $\overline{\text{RAM}}$ signal is delayed until the address is settled.

111. The decoded $\overline{\text{RAM}}$ instruction at LK1 pin 2 is taken to IC12 D1 input (pin 2). IC12 is clocked by the rising edge of the CLK (pin 3), this will occur when the address bus (and $\overline{\text{RAM}}$) are stable. The Q1 output of the first flip-flop (pin 5) is taken to IC16 (pin 17) octal buffer.

112. The second flip-flop of IC12 will subsequently be clocked at the end of the read or write cycle via IC4d and IC2d for which the $\overline{\text{RAM}}$ was asserted by the rising edge of either $\overline{\text{WR}}$ or $\overline{\text{RD}}$ signals. This clocks '0' into Q2 output (pin 9) which sets Q1 output (pin 5) to '1' asserting $\overline{\text{RAM}}$ 'high', see Fig. 11. Flip flop 2 is preset to '1' when the ALE is returned to logical 'high' via IC2e.

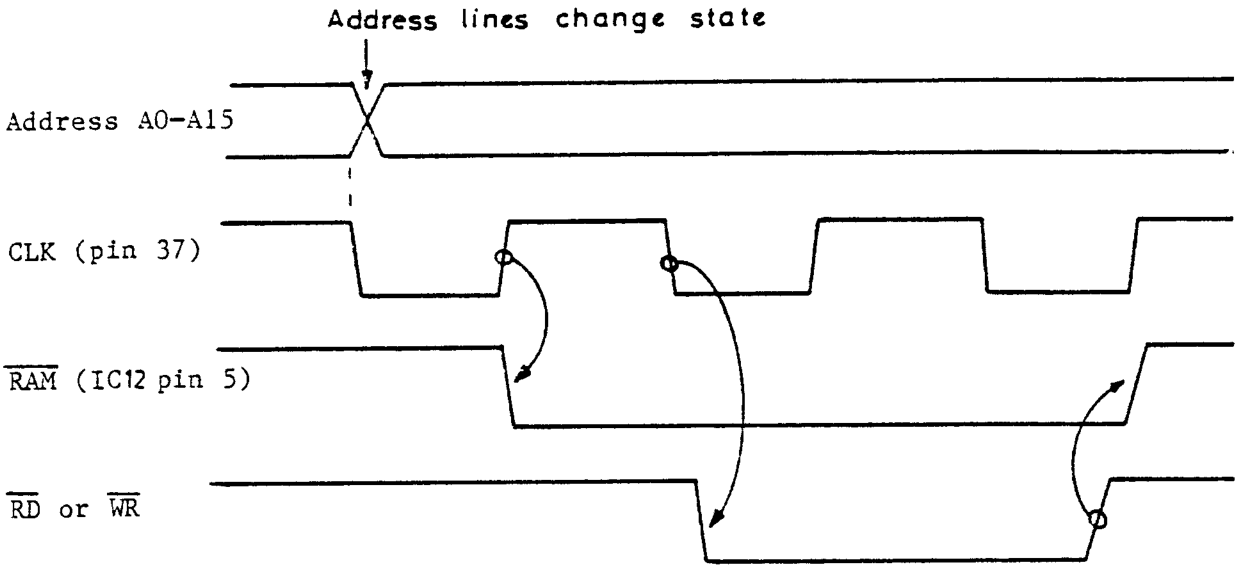


Fig. 11 RAM Select Timing waveforms (AC18)

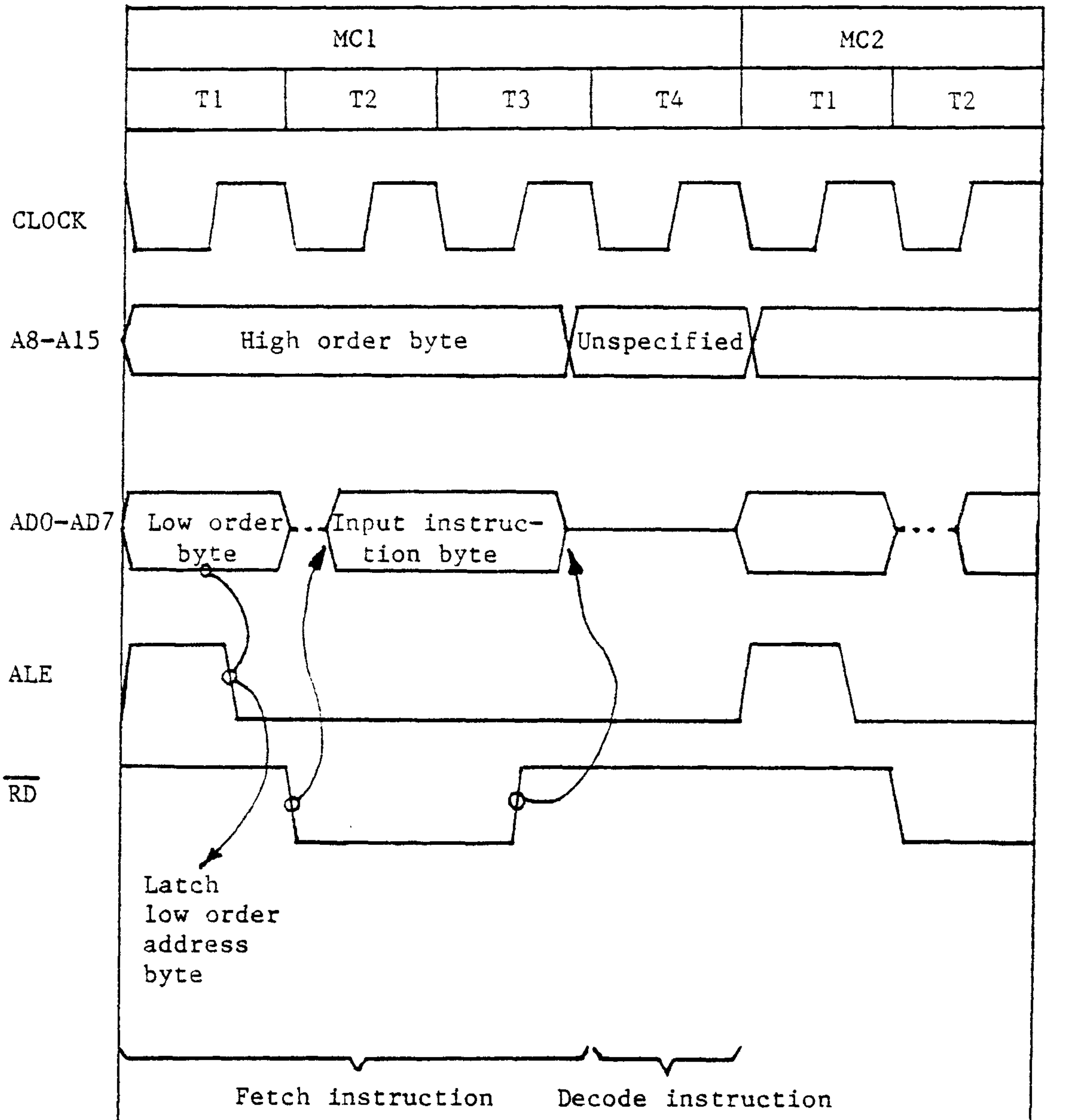
113. **READY instruction**, locations 8000H - 8FFFH are reserved for INPUT/OUTPUT ports thus simplifying decoding. IC13 Wait-on-port circuit operates when A12,A13 address lines are 'high' giving a logical 'high' READY instruction to IC1 pin 35. The operation of the CPU is directed into read and write sequences called Machine cycles. These may contain from 3 to 6 clock cycles (or T states) with the instruction fetch MC1 containing a mimimum of four T states and the remainder three.

114. Slower INPUT/OUTPUT devices require more time to respond therefore it is necessary to increase the length of the $\overline{WR}$ or $\overline{RD}$ signal. Provision for this is made by the ability of the CPU to generate a 'Wait clock period'. The READY signal line is sampled by the CPU at the clock period T2, if this is at logical 'low' a Wait clock period will follow, further Wait clock periods would be generated until the READY signal line is asserted 'high'. One Wait clock period only is required by 6500, the clock periods and signals generated in the first machine cycle are shown in Fig. 12. IC13 'Wait-on-port' circuit holds the READY line 'low' for one count (approx. 200 ns) then asserts 'high', the next clock period T3 then follows.

115. A $\overline{PRT}$ ($\overline{PORT}$) signal is derived when either $\overline{RD}$ or $\overline{WR}$ lines are gated with A12,A13, address lines via IC3b, IC4a, IC4b and then buffered by IC16. $\overline{PRT}$ is asserted low whenever a port (address 8000H - 8FFFH) is accessed for either a read or write operation. Timing requirements cause some noise spikes on the output latched address lines, these are caused during the transition from Data to Address and are to be expected.

116. **Read operations**, the 6116 type ICs have two control inputs $\overline{CS}$ (pin 18) and $\overline{WE}$ (pin 21). Each of the ICs I/O pins (9 - 17) are effectively disconnected from the system bus when $\overline{CS}$ is 'high'. When $\overline{CS}$ is asserted 'low' one of the IC pairs are enabled and the $\overline{WE}$ ($\overline{MEMW}$) signal determines whether a Read or Write operation is to be performed. When $\overline{WE}$ is 'high' and $\overline{CS}$ 'low' the 6116 will output the addressed read data to the system data bus.

Fetch instruction machine cycle



The wait clock period

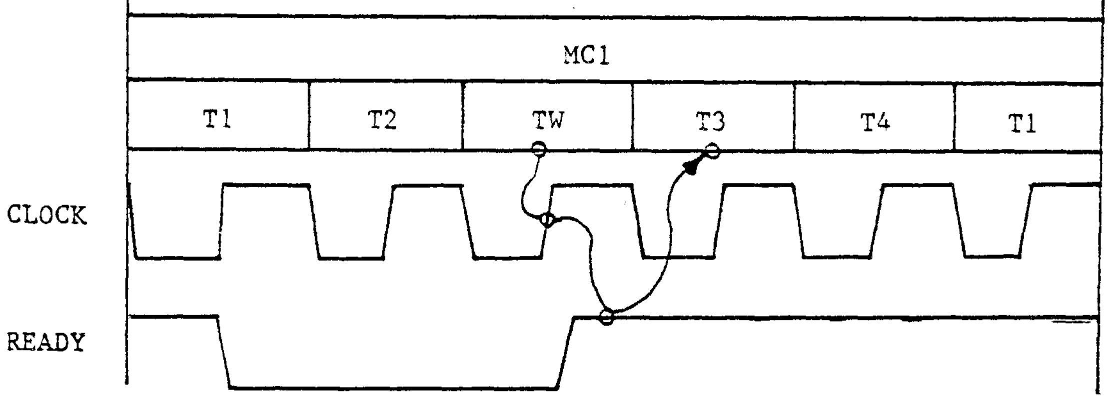


Fig. 12 Machine cycle Wait state and Fetch instruction (AC18)

117. **Write operations**, a write operation requires both the $\overline{CS}$ and $\overline{WE}$ ($\overline{MEMW}$) signals to be asserted 'low' to the point where the earlier of the two goes 'high' again. Addresses must remain stable for the entire write cycle although data inputs may change. The data inputs which are stable during DATA IN period at the end of the write time will be written into the addressed location.

(1) **RAM testing.** A self test is carried out at power on. All RAM is cleared to '0' and all RAM is given a non-destructive chequer board pattern test. That is to write and read 0AAH and 055H. This test does not check for decoding errors or pattern sensitivity errors, but is fast. Should that test fail LOCAL and SHIFT l.e.d's will flash alternately and an indication of the fault will be shown (see Operating Manual, Chap. 3-1 for details).

(2) **EPROM testing.** A checksum test is also performed on all EPROMs at power on as part of the SELF TEST. A checksum byte is set to zero at assembly time. A special loader program replaces this byte with a value which results in a checksum of zero. The checksum is the sum of all bytes in the EPROM evaluated modulo 256.

(3) A RAM test also runs continuously in the background during instrument operation. The test is activated every time the delay routine is called. A pointer is maintained to indicate where the test should resume when the delay routine is next activated.

Software Link options (AC18)

118. To enable increased versatility, three Link options are fitted to this board allowing further expansion of address space and the selection of an integral diagnostic ROM. IC5 decodes four 2 K RAM select lines for IC17,18,19,20 mapping the 8 K RAM into the upper half of the 16 K block specified by $\overline{RAM}$.

119. IC6 decodes the lower 32 K of address space in 4 K blocks, pairs of which are gated by IC21 AND gates to give 8 K block select signals for EPROMs IC7,8,9,10. Link 2 allows the upper 4 K of IC9 to be deselected when operating in unexpanded mode to prevent conflict with the display generators located at 5000H to 5FFFH. Link 3 allows IC10 to be mapped at 6000H - 7FFFH (expanded operation), or permits its use as an integral diagnostic ROM located at 0000H should Link 4 be placed into the TEST position. Link 1 selects the $\overline{RAM}$ block for either NORMAL (4000H - 7FFFH) or EXPANDED (C000H - FFFFH) operation.

120. **Option One**, this option enables the user to operate with earlier issues of Software (up to Issue 4) with the four links fitted in the positions shown below. The resulting Memory map configuration is also shown in Fig. 13.

LK1 pins 2 & 3 connected, (NORMAL OPERATION)
LK2 pins 1 & 2 not connected.
LK3 pins 2 & 3 connected, (NORMAL OPERATION)
LK4 pins 2 & 3 connected, (NORMAL OPERATION)
LK4 pins 1 & 2 connected, (TEST: in this position diagnostic ROM is selected at location 0000H - 1FFFH in lieu of $\overline{ROM\ 0}$).

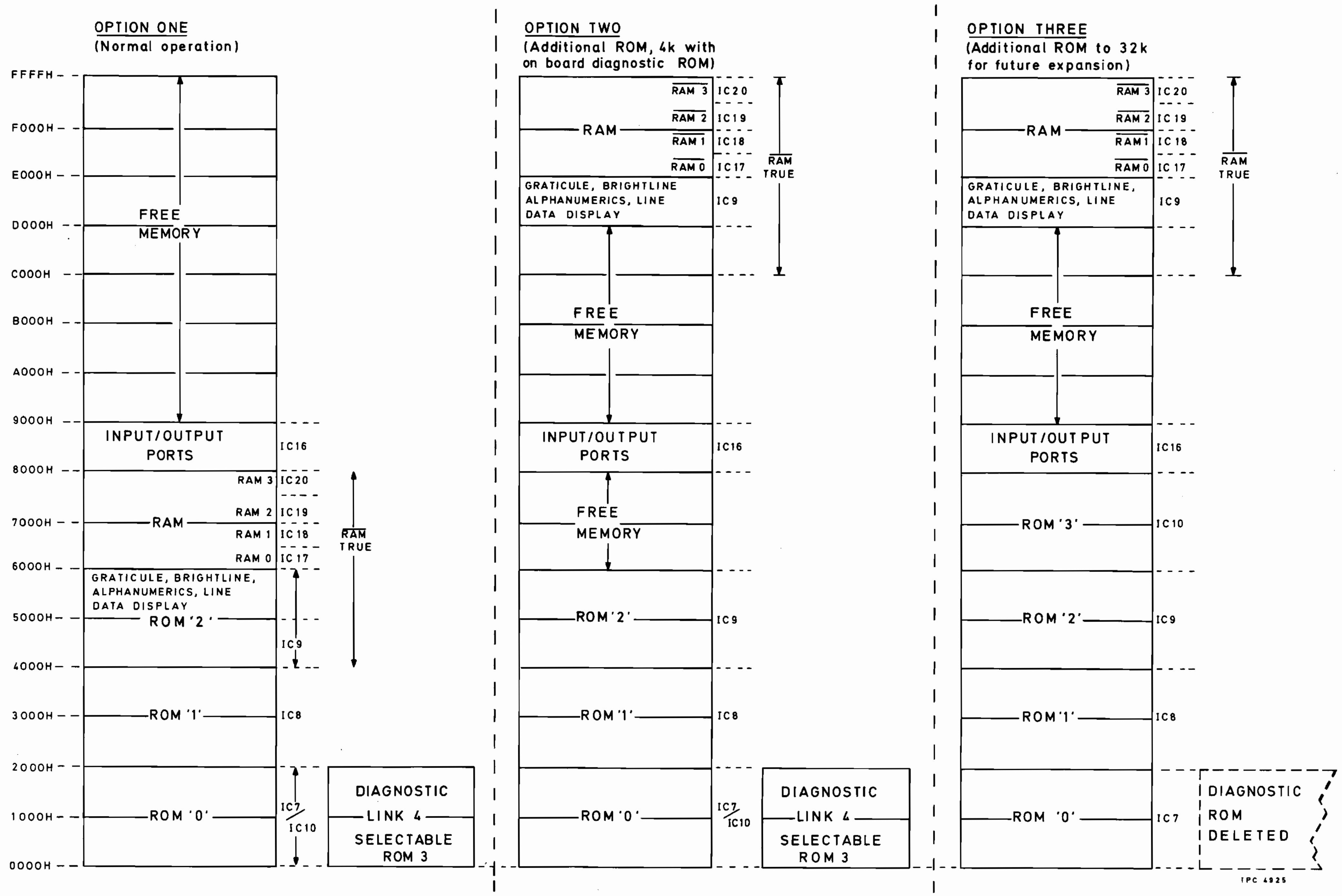


Fig. 13 Link options memory map (AC18)

121. **Option Two** (Expanded ROM to 24K), in this configuration Links 1 and 2 when connected to EXP, access an additional 4K of ROM via IC9 (deselected in NORMAL mode). Link 4 can be positioned as shown in Option one.

LK1 pins 1 & 2 connected, (EXPANDED OPERATION)
LK2 pins 1 & 2 connected. (EXPANDED OPERATION)
LK3 pins 2 & 3 connected, (NORMAL OPERATION)
LK4 (as for Option one).

122. **Option Three** (Additional ROM to 32K), this option allows for future expansion which has not yet been introduced. Up to 32K of ROM could be utilized in this configuration if the diagnostic ROM is deleted.

LK1 pins 1 & 2 connected (EXPANDED OPERATION)
LK2 pins 1 & 2 connected (EXPANDED OPERATION)
LK3 pins 1 & 2 connected (EXPANDED OPERATION)
LK4 pins 2 & 3 connected (NORMAL OPERATION)

In-Out Board (AC09/2)

Circuit diagram : Chap. 7, Fig. 6

123. The function of this board is to provide the X Ramp; X Plotter; Y Plotter; Auto zero and Null voltages, these are all controlled by the microprocessor. Other functions include the SYNC sensing circuit, the output of which is fed to a port. Another port is provided for the control of the plotter, providing the pen-lift control and disabling the plotter drives when this facility is not being utilized. Decoding for the GPIB board memory map also takes place on this board. If the microprocessor is not running, no control of any of the above mentioned functions is possible.

124. Decoding of memory map locations is provided by IC2, the board being selected when PRT (port enable) line is low and A10 high. IC3 decodes two Device select lines used on the GPIB board; these are, the 8291A SELECT active ´low´ signal at pin B6, and GPIB SW active ´high´ at pin B7, both are decoded on this board so as to limit the number of lines to be taken to the GPIB option. This reduces the possibility of pick-up and also allows the option to be used without modification in conjunction with other instruments where the address may be different.

125. Four Digital-to-Analogue converters (DACs) are used on this board, two standard 8-bit ZN 425E and two 12-bit AD 7542. All have the analogue voltage output adjusted by Operational amplifiers to the required level and range.

126. AUTO-NULL DAC, this comprises IC6, latch, IC7, DAC, and IC8a, Op-amp giving ≈ ±2.5 V analogue output depending on the data written to the latch. This output is fed to AC12 and is used to adjust the signal channel performance and enhance the accuracy. The output is adjusted during the AUTO-ZERO operation, one set of adjustments per range, per channel. Successive approximations are made until the ´correct´ voltage is reached, i.e. the most significant bit (MSB) will be toggled, then each bit in sequence, down to the LSB, after each adjustment AC12 will be analyzed by the microprocessor. A table of null data is held by the microprocessor and the correct value is selected as the ranges are altered to suit the signal level and/or channel selected. In calculating each bit a series of readings (without correction) are taken. Each is compared with an ideal ´floor´ value corresponding to the lowest entry in the Log conversion table. Since there is considerable noise present at this low power level, averaging of many readings is required. Since the log table is non-linear the effect of averaging many readings is to create an artificially high value. A weighting system is employed to avoid this. Readings above the ´floor´ value are assigned a weight of ´1´ and those equal to the ´floor´ value ´0´. The weighting values and not the ADC readings are then averaged and the status of the current bit in the successive approximation is dependent on whether the result is greater than 0.5. Nulling operations assume that no r.f. power is applied. A check is made for a detector present by reading the temperature sensor.

127. Y-RAMP/PLOTTER DRIVE. In a similar way to the circuit described above IC9 latch, IC10 DAC, and 1/2 IC8b provides an analogue voltage output during the PLOT mode. In this mode of operation the PLOTTER Y DRIVE output at pin PL3-4 is 0-10 V and R9 provides the adjustment of the plotter Y-Ramp full-scale deflection.

128. **X-RAMP/PLOTTER DRIVE.** IC14 is a 12-bit DAC compatible with the microprocessor and has 3 internal 4-bit registers, Most significant, Middle, Least significant and a latch (or conversion enable). The microprocessor writes in the required digital code and when complete, strobes the latch register - which in turn makes the conversion. The register addressed is determined by address lines A0 and A1 applied to IC14 pins 10 and 11, the output current drawn by IC14 pins 1 and 2 is then converted to a voltage by IC15.

129. IC14 is a multiplying (inverting) DAC with a reference voltage derived by IC11a and D4 which together provide a -10 V reference, pre-set by R12. D4 is a -6.2 V Zener and R13 provides the correct bias. Capacitors C22-C26 ensure a noise free reference. The analogue voltage at IC15 pin 6 is fed to the Ramp output via PL1 and through relay RL1 to PL3-1 (Plotter X drive).

130. When the PLOT mode is not in use RL1 is de-energized to prevent spurious plotter operation. This is controlled by IC5 and TR1, pen-lift is also controlled by IC5 via R28 and TR2. TR2 is a high power Darlington transistor and is used here because high voltages can be returned from some X Y Plotters (from the pen-lift relay).

131. **AUTO ZERO DAC.** IC12 DAC requires 4 ports and occupies a contiguous address space 8204H to 8207H. Operation is similar to that of IC14 and the same -6.2 V reference voltage is used together with IC12b to give a +11 V reference at IC12 pin 15. Current drawn by IC12 pins 1 and 2 is then converted by IC13 to a voltage output in the range 0 to -11 V and fed to pin B1. A correctly zeroed display will show noise (grass) at an approximate level of between -60 and -50 dBm. Incorrectly fed voltage will result in the display showing a lower or higher reading - possibly a flat line <-60 dBm or noise around -45 dBm or higher. The voltage output at pin B1 in AUTO ZERO mode is approximately -3 V and -4 V determined by R16 connected to IC11b (-6.2 V reference). The zero value is calculated for each of the three chopper amplifiers. The Autozero routine calculates a table of values which are referenced whenever the input channel of the signal processing system is changed.

132. **SYNC INPUT DETECTOR.** IC16 detects the 'high' >+2.5 V, and 'low' <-2.5 V inputs at PL3-5, this is fed in from the rear panel SYNC socket. The detected output is then applied via IC1b,c to the data bus line D0. IC1b,c comprises two tri-state buffers which are enabled by IC2 pin 7 asserting logical 'low' to select this port.

133. During normal operating conditions the X Ramp is used to drive an external sweeper over all or part of its frequency range. In practice a set of values is obtained/calculated in the RAM store as set by the F1, F2, START and STOP figures, entered by means of the keyboard. F1 corresponds to 0 V (0000H) and F2 to 10 V (FFFH) hence F1 <START <STOP <F2.

134. As the 6500 sweeps from START to STOP a value is read from memory corresponding to the position of update across the screen (0-421 positions), this is sent to IC14 DAC before the measurement is made at each successive point.

A-D system and log conversion (AC11)

Circuit diagram : Chap. 7, Fig. 7

135. The function of this board is to provide the analogue-to-digital conversion on a 0-10 V signal input. The microprocessor reads data from this board in log form converted by two look-up Log PROMS rather than in linear form. With an input signal of 10 V, data of 0 dB is read, with a 1 V input, data of -10 dB is read etc.

136. Because the log table contained in the PROMS is compressed near the upper limits (log law), a Range shifting circuit is used allowing all the data to be included in just two PROMs.

137. The board also contains the latch for the control lines used by the Signal channel (AC12 and AF03/1 boards) for channel and gain selection and for enabling temperature measurements. These are mounted on this board to prevent digital noise created on the microprocessor bus from being injected into the signal processing stages. The ADC Status port IC20 provides information re the conversion - whether valid, top-of-range, bottom-of-range so that necessary corrections can be made if required to the Signal channel gain settings, i.e.

1. Conversion complete.
2. Out-of-range - indicates ADC output word is outside the desired limits.
3. Under/over - Indicates whether gain should be increased or decreased by 10 dB.

138. To ensure accurate operation, the A-D converter is only operated over 90% of its range (10 V to 1 V, or 0 dB to -10 dB) preventing large quantization errors in log conversion below this.

139. The 'bottom-of-range' detect is a 12-bit comparator detecting conversions of values below -12 dB; as each gain stage is a factor of 10 difference in gain, this results in a 2 dB overlap between ranges. The 'top-of-range' detect selection is performed by OR gates detecting all '0's (the ADC-80 is inverting).

140. IC3 is a 12-bit (ADC-80) successive approximation A-D converter which is capable of performing a full 12-bit conversion in ≈ 26 µs. The speed is such that the conversion is performed without the need for a sample-and-hold circuit (the time is of the same order as the 'free' time in the chopper cycle, for details see AC12 paragraphs).

141. IC3 could cause unwanted fast switching spikes to be fed back through a common supply line to affect the highly sensitive chopper amplifier circuits on board AC12. This possibility is avoided by supplying board AC11 with separate ±15 V digital supplies.

142. The signal input is first buffered on board AC12 and then fed via pin A7 to IC3. A CONVert, conversion pulse of approximately 1 μs duration (free running without microprocessor intervention) is derived from AC12 chopper drive signals fm/2 (7.8 kHz) and is applied to IC3 via pin A10 and IC13d, to initiate each conversion.

143. It takes approximately 26 μs to carry out the 12 bit data conversion. On completion an END OF CONVERSION (STATUS) pulse is set at pin 22 which is fed to IC20 ADC status port. The microprocessor tests the status port to determine when a conversion is complete. The data read must be completed within 38 μs, before a further conversion takes place. Decoupling capacitors C8, C9, C4, C5, prevent current glitches from causing interference on the Signal channel.

144. Top-of-range/Bottom-of-range detects, IC7, IC8 and IC9 form a 12-bit comparator looking for a value from the A-D converter corresponding to -12 dB (or less) indicating that the current selected range has insufficient gain. If this is confirmed a signal is fed to IC20 pin 6, or pin 4 (via IC13b). This signal is coupled with a Top-of-range signal generated by IC11,IC12,IC13, when all IC3 data outputs read zero (indicating that a range change is required). The two signals combine at IC20, the UP/DOWN signal determining in which direction the range is to change.

145. Log data PROMs IC18/IC19. To compress the log data contained in these PROMs and maintain similar resolution throughout the 0-10 dB range, IC4,IC5,IC6 and IC14,IC15,IC16 perform two separate resolution shifts by adjusting which of the ADC bits address the Log PROMs. This depends on where in the range the data is and is necessary to prevent visual degradation of the signal over the 10 dB range.

146. Consider the memory map shown in Fig. 14, in the area (1), due to the high resolution data at adjacent points would be almost identical. Because of this only the most significant 10-bits of the ADC's output data are used. Address lines A2-A10 are routed via Range/Resolution Shift 1 'B' inputs and then IC14-IC16 'A' inputs to the EPROM IC18/IC19. Address line AD11 controls IC4-IC6 (via IC10c), AD10 and AD11 lines together control IC14-IC16 (via IC10a) and IC18,IC19 (via IC10a,IC10b) to give an EPROM address once every four ADC counts.

147. In area (2) address line AD11 directly controls IC4-IC6 and the 'A' inputs carrying lines AD1-AD9 are routed through to IC14-IC16 'A' inputs to give an EPROM address once every two ADC counts.

148. In area (3) when both AD10 and AD11 address lines are logic 'high' (IC3 is an inverting ADC), the address lines AD0-AD9 are connected directly to the 'B' inputs of the second Range/Resolution Shift multiplexer IC14-IC16. This gives an EPROM address on every ADC count.

149. IC18 contains the most significant byte (MSB) of each of the 16-bit log values. IC19 contains the least significant byte (LSB). The two ports are located in the Memory map at adjacent locations enabling a fast double byte load by the microprocessor. IC18 and IC19 are permanently selected, and only the output enable pin is pulsed when selected. IC22 provides the memory map decoding for the board enabling the reading of LSB, MSB and STATUS, and writing of a control byte to IC21, Range and multiplex latch.

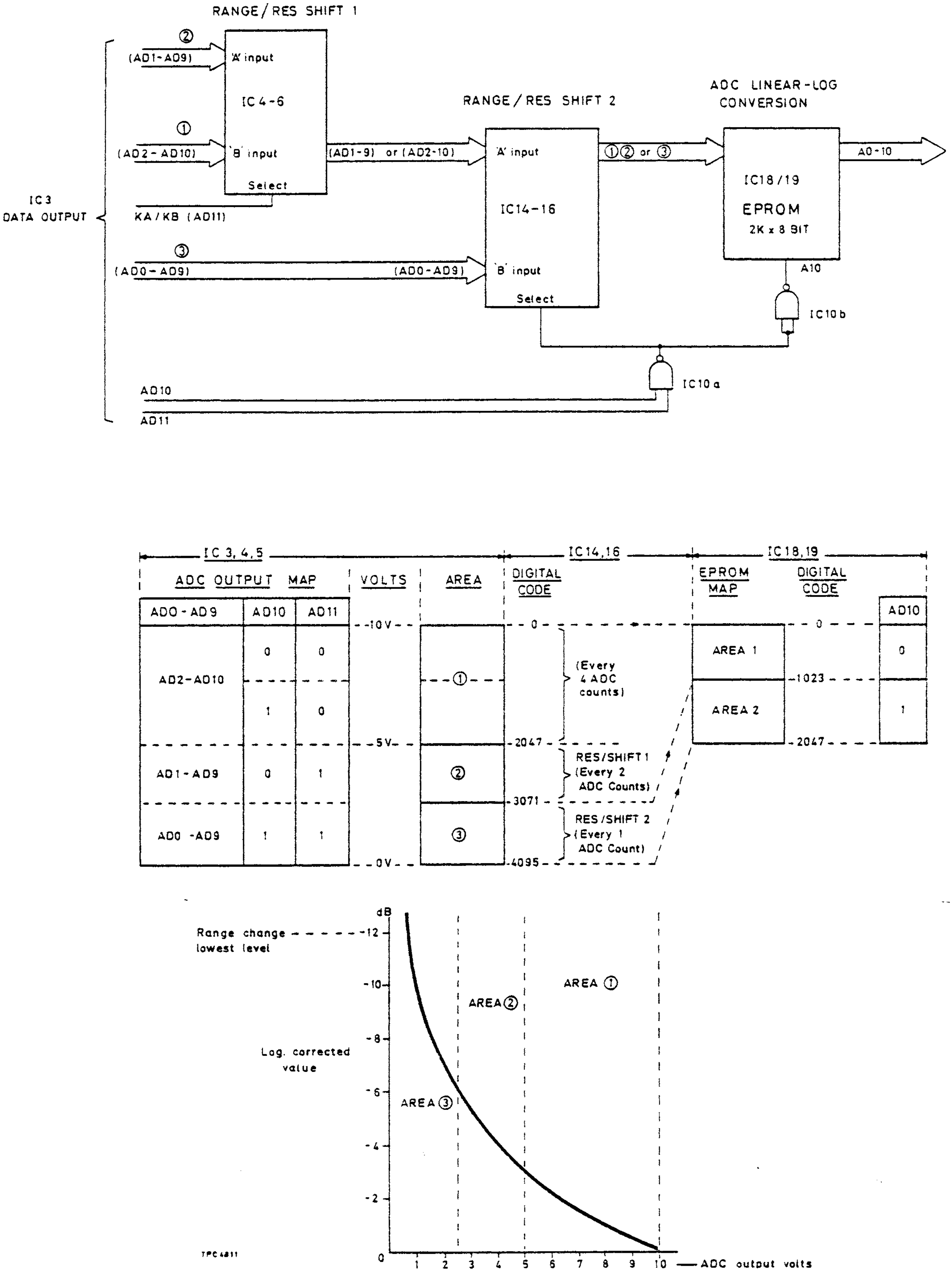


Fig. 14 Log data PROM Range/Resolution (AC11)

Signal channel (AC12 & AF03/1)

Circuit diagrams : Chap. 7, Figs. 8 & 11

150. The three signal channels A,B and R are combined on the two boards AC12 and AF03/1 and are described in this section together for convenience. AF03/1 board is mounted directly behind the instrument's input sockets to ensure the least possible noise pick-up from coupling wires and connectors, AF03/1 also provides the initial amplification and temperature sensor detection.

151. The detectors used will provide a voltage output in the range 1μV to <2V to cover the dynamic range of the instrument. In the lower voltage output region the output will be proportional to the incident power this is known as the square law region, as input power $\equiv Pi \propto Vi^2 \propto Vo$.

152. The detectors provide only a d.c. signal which is carried from the detector on two lines (a third, earth line is also used as a voltage reference point), both d.c. signal lines are taken to high impedance inputs with the shortest interconnections possible, otherwise current returns generated would create a voltage which would completely swamp the signal at low levels. An f.e.t. chopper circuit has been used to provide the high gain stability required, any instabilities being limited to a.c. gain/shape variations which can be minimized and corrected for in later stages.

153. If a sweep speed of 100 ms is selected each of the 422 measurements covering all 422 measurement points must be completed in approximately 250 μs, therefore at least one cycle of the chopper is necessary to achieve a good response. The speed of the chopper then should be greater than 4 kHz. However in order to reduce the inherent noise and pick-up from the adjacent c.r.t. radiation at line frequency (15.625 Hz) the chopper has been synchronized to half this (7.8 kHz) to provide the required speed and at the same time minimize the effects of c.r.t. scanning radiation by being synchronous with it.

154. Signal processing is controlled by the microprocessor via an 8 bit port, (SET GAIN, location 8804). Three stages, each of which may be switched to either high or low gain give six 10 dB range selections. A three bit signal specifies selection of each of the three measurement channels, A,B,R or optionally selects the detector temperature sensor for that channel. A further 3 bit signal is used for gain switching. The gain is programmed by setting combinations of these bits to select the range that will maintain an output voltage between 1-10 V. Range switching is requested by hardware on AC11 board.

155. The f.e.t. choppers generate a p-p a.c. signal equal to the level of the detector d.c. which is fed to the first stage amplifier. This is preceded by a switchable ÷100 attenuator to provide the first gain select switch. All three channels, identical up to this point are then connected to a multiplexer from which a single output is buffered and fed to AC12 board for further processing.

156. A temperature sensor mounted in the detector head provides data for temperature correction. The sensor comprises a simple base-emitter junction and is biased via a constant current to give a specific voltage at a specific temperature. The coefficient of this junction voltage is used to sense the temperature variations and AF03/1 temperature sensor circuit gives an arbitrary, but consistent output voltage from which the actual temperature can

be determined by a calibrated table held in the microprocessor memory. The switching of this is carried out on AC12 and the output is applied to the main ADC, IC3 on board AC11. Figs. 3 and 4 show the overall set-up.

157. The signal output from AF03/1 is coupled to AC12 via SK1 and SK2, a deglitch circuit at the output of AC12 prevents noise spikes previously generated by the f.e.t. chopper from either limiting the gain stages or being integrated with the signal. These noise spikes are instead removed by the action of AC12 (IC9) which acts as a sample and hold, holding the voltage present just before the spike occurs to a fixed level throughout the duration of the spike.

158. Two further stages of amplification are employed, the 2nd stage amplifier IC1 provides xA and x100A gain and the 3rd stage amplifier IC3 xB and x10B gain. The a.c. signal is restored to d.c. by a phase synchronous detector. A further sample and hold circuit operates synchronously with the chopper circuit and takes a small sample of each half cycle of the chopper waveform and maintains this voltage on a capacitor, the difference being detected by an instrumentation amplifier to provide a d.c. signal. The signal is then summed with a Null voltage which is calculated by the microprocessor when an AUTO ZERO operation is correctly performed. This operation is necessary because different R-C time constants on different ranges affect the a.c. signal's shape and must be corrected for.

159. When null values are correctly calculated the output of the DC amplifier stage with no incident power on the detector will be 0 V. The signal output is finally switched by a multiplexer and buffered to provide both signal and temperature voltages to be applied to the A-D converter on board AC11. The signal is also clamped to prevent negative excursions from damaging the ADC.

160. Board description (AF03/1). The circuit diagram illustrates only one of the three 1st stage amplifier circuits actually fitted. 'A' channel shown on the circuit has component numbers in the series 100-199. 'B' and 'R' channels are identical and have for convenience been omitted from the circuit, 'B' channel components are referenced in the series 200-299 and its output is connected to IC1 pin 5. R channel components are referenced 300-399 and its output is connected to IC1 pin 6.

161. Chopper and 1st stage Amplifier, TR101 and TR102 form a series/shunt f.e.t. chopper. The drive signals to the gates are fed via R124,R125,R128 from IC3 and IC4. IC3 buffers and IC4 inverts the chopper control signals when channels are selected so that the f.e.t.s are alternately switched on. The two control lines (f.m.1 and f.m.2) are generated on AC12, the signals having a specific phase relationship to each other. This ensures that a pre-determined on/off sequence will occur on the f.e.t.s.

162. When 'A' channel is not selected, TR101 will remain open circuit and TR102 short circuit. The stopping of the chopper prevents breakthrough and possible saturation of unused amplifiers. The selection of Channel A is carried out by the gating of f.m.1 and f.m.2. R124 and R125 prevent current spikes from being introduced by limiting the available current.

163. R128 ensures that the logic 'high' (on) voltage does not exceed ≈ -1.3 V (At high power levels the detector could produce a voltage exceeding -1.5 V to forward bias the series f.e.t. and cause breakthrough at the chopper frequency). The junction of R103/TR102 is the point used for injection of a voltage to counteract small offset voltages present due to pick-up and chopper

spikes. This is the AUTO-ZERO voltage and is applied via PL1 pin 3 and is derived on board AC09/2, see paragraph Y-Ramp/Autozero/Plotter drive for details.

164. R101 protects TR101 when no detector probe is connected and acts as the standard load when one is fitted. The chopper earth reference (STAR POINT 1) is starred on the p.c.b. to prevent induced voltages from producing erroneous signals. D103/D104 prevent the OVA chassis ground and STAR POINT 1 from varying by more than ≈ 0.5 V. All signal path returns are high impedance to reduce induced d.c. offsets. C101 a.c. couples the signal to the attenuator and 1st stage amplifier, the time constant C101/R126 ≈ ms is chosen to give optimum signal transfer without degradation of the low frequency response which would appear as a slope on the signal. This would result in an accuracy or noise error. C109 removes r.f. pick up by the detector probe cable protecting the 1st Stage gain amplifier from saturation.

165. IC102 is a digitally controlled dual, single pole changeover switch and selects either the entire signal if switched to one of the ranges 3 to 6, or for signals of higher power levels selects the ÷100 attenuator. The output of IC102 is fed to the base of TR103, the base resistor being formed by the attenuator when selected. A constant current flows through the base, therefore a different d.c. voltage is generated at the base when the attenuator is switched in. For these reasons the value of base resistance should not fall below ≈1 kΩ. When ÷100 is selected R126 is placed in series and produces a time constant coupled with parasitic capacitance on IC102 which affects the shape of the signal. This can be countered by adjustment of R105.

166. The first gain stage, TR103 (a specially selected low noise device) and IC101 give a voltage gain of ≈300. R112,R109,R106 and R115,R108 form bias chains defining the current flow through TR103. Gain of the stage is determined by R119, R116 and R107 forming a feedback loop, and C103,R107, defines the low frequency response. High frequency response is decreased by C111 reducing some signal noise. This in turn will widen the chopper spikes to some extent, but this effect must be minimal or the integrated chopper spikes will affect accuracy and drift performance. The value of C111 is therefore empirically calculated. R110 and C104 form a d.c. feedback path preventing the effects of temperature variations. C102 and C110 give protection against radio frequency interference.

167. The overall gain of all three channels A,B and R are set to identical levels adjusting R119,R219 or R319 respectively, see Chap. 5, Maintenance for details. This amplifier typically provides gain of ≈300 and the noise performance is such that at ≈30 dBm on the 6500. there is ≈0.1 dB p-p noise. As the 20 dB attenuator switches at about -15 dBm the noise figure at -10 dB is similar.

168. IC1 multiplexes the three inputs to give a single output signal controlled at pins 1 and 16. Multiplex control lines M0 and M1 determine which signal is to be selected and which chopper will be driven. The temperature sensor is also controlled by these lines via IC5. Output from IC1 pins 3 and 8 is buffered by the unity gain IC2 where C3 and C4 decouple large current glitches when driving into AC12.

169. TR1,R15,R16 form a simple inverter to drive the 1st stage attenuator switch IC102, this is driven by the RO line (PL1/6) from AC11(A3) when instructed from the microprocessor. C6 and C7 remove noise from the ±15 V supply lines, C10 reduces pick-up noise from the AC09/2 Auto-zero voltage line. IC7,C8,C6 form a +5 V regulator which is referenced to 0 VA. This has the effect of decreasing ground noise significantly and isolating the digital lines from the 0 VA line.

170. <u>Temperature sensor unit</u>, this circuit provides a temperature dependent voltage ∝ temperature. A temperature sensor (base emitter junction) is bonded near to the diode within the detector probe. The junction responds to a temperature change by a linear change in voltage when biased with a constant current. The constant current is provided by D1,R5,R9, R5 being selected depending on the actual Zener voltage of D1 which can vary by 5%. This then ensures a constant current within 2%. R7,R8,R10 sets the reference voltage for IC6 pin 2 and the required gain necessary to cover a 0-50^{0}C temperature range is provided by R8.

171. Calibration at a simulated 22^{0}C is performed via R6 which adjusts the offset voltage. The overall gain is set to ≈70 with the voltage set within the region 0-10 V. This voltage can be selected to read by the microprocessor using the main ADC(AC11) by a switch (AC12,IC12 multiplexer). The output at PL1/7 is routed to board AC12, C11 reduces noise on the signal whilst still maintaining a reasonsably fast response when channels are switched over. A stable output within 1 ms is required.

172. <u>Board description (AC12)</u>. The a.c. input signal from A,B or R channel is fed from AF03/1 via SK2 to the de-glitch switch IC9 pin 4. IC9 removes the chopper spikes developed on AF03/1 by becoming high impedance during the time that these are generated - the voltage is held on C5. Control of IC9 is achieved by a DE-GLITCH(HOLD) control pulse applied at pin 2, this opens the switch when the majority of the spike has finished allowing 'live' signal to pass through to IC16. (Actual detection and conversion of the signal is carried out by sampling and holding 'live', not de-glitched signal). The voltage on C5 appears as a horizontal line during the glitch, as the time constant of C5 and the input impedance of IC16 is of the order of seconds. The resultant output is such that the glitch is switched out and the signal effectively phase shifted. The charge on C5 does not then reflect the glitch as shown in Fig. 15.

173. The value of capacitor C5 has been chosen to allow the buffer stage of AF03/1 to charge it up sufficiently quickly without creating distortions due to current limiting. However, the de-glitch itself produces another charge glitch which is added to the charge on this capacitor, and if the capacitance is too small an error occurs due to shifting of the voltage by the injected charge.

174. IC1 and associated components form the 2nd stage amplifier. IC2,R6 allow operation at a lower gain. R2/C2, and R3/C3 filter the ±15 V supply and R1 minimizes noise by equalizing the input currents. Gain of the stage is controlled by the microprocessor deriving the R1 signal on board AC11(IC21), this is fed via pin (A2) to IC2 pin 2. When R1 is at logic '0' R6 is connected across R4/R5 reducing the gain by a factor of 100. The output of the 2nd stage amplifier is prevented from reaching the common mode input voltage rating of the next stage by D2/D3 which limit the output to 8.2 V.

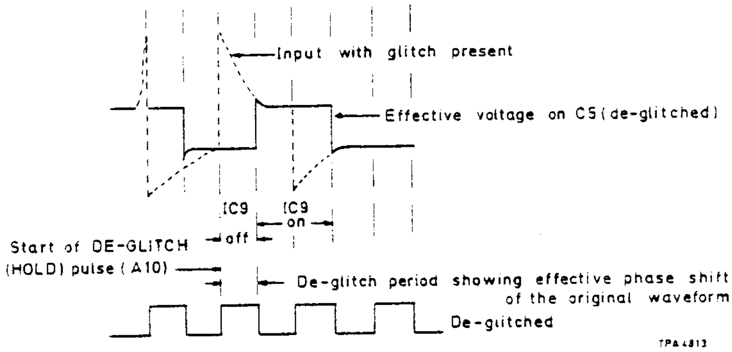


Fig. 15 Deglitched input to AC12 2nd stage amplifier

175. The 3rd stage amplifier IC3 is similar to the 2nd stage and provides either approximately x10 or unity gain. Control is achieved by the R2 signal at pin A1, also derived on board AC11(IC21), this is connected to IC2 pin 1 and when at logic '0' connects R15 across R13/R14 reducing the stage gain by a factor of 10. Signal output level from this stage should be between 2 V and 10 V p-p when the range/gains are correctly selected. Both IC1 and IC3 amplifiers must have a high slew rate performance and are OP-01 low noise inverting type.

176. **Phase synchronous detector**, the input a.c. signal is restored to d.c. by this circuit so that it may be combined with (NULL) correction voltages and switched to the ADC. Samples of the signal are taken on each half cycle by closing the switches on IC4 alternately, with C13 and C14 charging up to the sample voltage during the time the switch is closed. See Fig. 16, these sample and hold capacitors must be able to charge and discharge rapidly to enable small details in a measurement to be faithfully transposed on the displayed output. The time constant is determined by the effective impedance of the switch and the output of IC3 and the value of C13 and C14. Together these allow an almost complete sample (up to 98%) to be obtained within the sample period.

177. IC5 acts as an instrumentation amplifier and offers high impedance to C13 and C14 so maintaining their charge and allowing a shift of earth reference to the OVD reference (OVD is the same ground reference as is used on AC11,ADC). Precision resistors R27-R30 ensure that the gain on each mode is the same, linearity errors would result if these differed. Overall sensitivity of the signal channel is adjusted by R33 and the signal is then mixed with the NULL signal (calculated by the microprocessor) by IC10a.

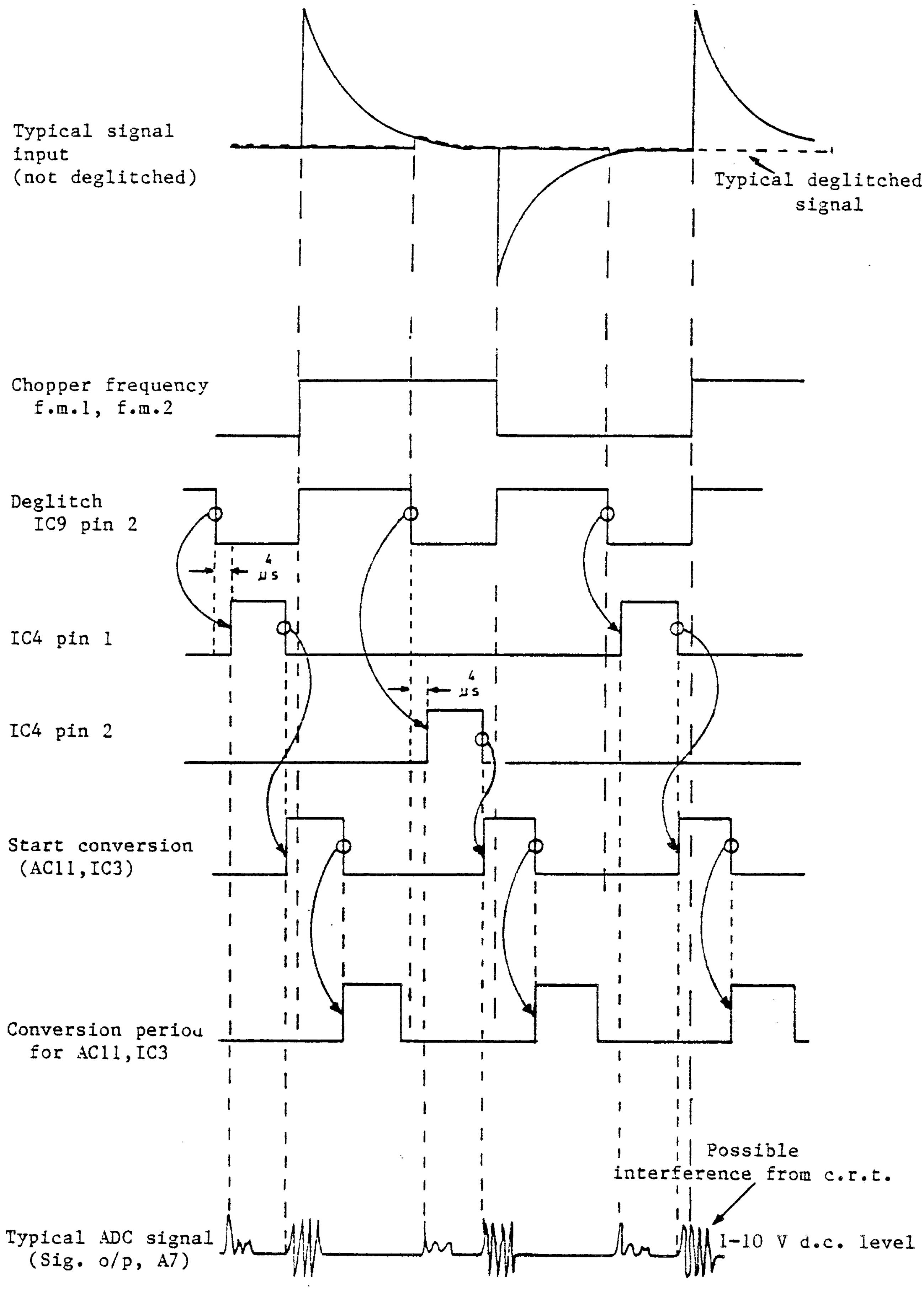


Fig. 16 Signal channel timing waveforms

178. Auto-null, Signal/Temperature circuits, the final signal will be 0V for zero r.f. input. Normal operation within a range will provide output volts of 1-10 V. This signal is fed to IC12 pin 4 and the temperature sensor voltage to IC12 pin 9. Either signal may be selected by the microprocessor with a T0 signal, initiated on AC11 and fed to AC12, IC12 via pin A4. R39 limits IC7a input especially if probes are not connected to AF03/1 when the voltage could rise to ≈13 or 14 V causing IC7a to malfunction.

179. R70 and D8 prevent excessive positive and negative voltage from being presented to AC11, IC3. The d.c. output at pin A7 is applied directly to IC3(the ADC) without smoothing - integration of sampling spikes being avoided by ensuring that the ADC conversion is synchronous with the chop rate. This also avoids interference from the c.r.t. line scan.

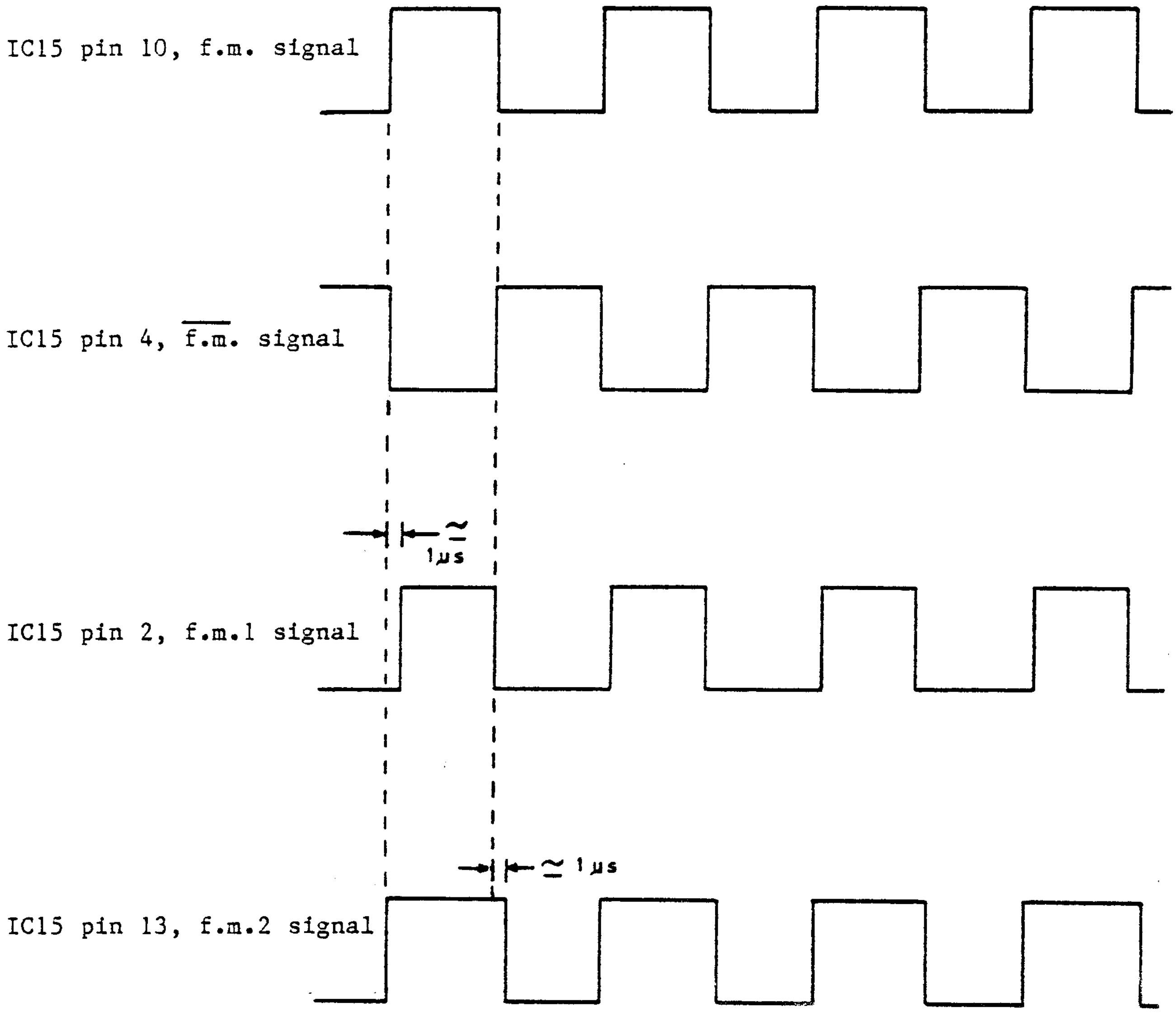


Fig. 17 Chopper drive signals f.m.1, f.m.2.

180. **Chopper drive**, the initial f.m.x2 line rate clock signal is derived on AC01(IC4 divider) and fed to TR5 buffer and inverter via pin A31. IC8 is a ÷2 divider and outputs f.m. and $\overline{\text{f.m.}}$ signals for use in the phase synchronous detector as described in previous paragraphs. Both f.m. and $\overline{\text{f.m.}}$ signals are also used to derive Chopper drive signals f.m.1 and f.m.2, for A,B, and R Channel selection on board AF03/1.

181. Both f.m. and $\overline{\text{f.m.}}$ positive-going rising edges are delayed at the input of IC15 by the action of C34, R52 and R53. Outputs at pins 2 and 13 are both positive-going at the same time with f.m.2 having the greater duration and leading the f.m.1 signal by a fractional amount. The difference in phase relationship ensures a pre/determined AF03/1 f.e.t. on/off sequence of operation. TR1 and TR2 are high current buffers and provide sufficient drive to the choppers to avoid the possibilities of pick up via the interconnecting ribbon connectors.

Ramp circuit (AR04/1)

Circuit diagram : Chap. 7, Fig. 15

182. Two ramp voltage outputs are available at rear panel sockets, a 0-10 V fixed voltage at SK5 and a 0-20 V variable voltage ramp at SK6. A ramp waveform is generated on AC09/2 and fed to the ramp smoothing circuit R13/C4, this removes any noise spikes. Buffer stage IC3a follows to give the fixed 0-10V ramp output at SK5.

183. 0-10 V REF input also from AC09/2 is applied via R14/C5 and buffer IC3b to give the required 0-20 V range, IC1a allows the adjustment of the top end of this range with both COARSE and FINE controls R4 and R6 and IC2, -12 V regulator stabilizes the output. The 0-20 V reference can be shifted by up to 10% of the total range by R5 OFFSET control.

184. Connections to the rear panel from AC09/2 are via a ribbon connector PL3 and coaxial connectors PL1 and PL2 to solder transition ST1 and SK1 and SK2.

Note ...

> In earlier models the above connections were made via SK13 of the motherboard AM01.

GPIB interface module

Circuit diagram : Chap. 7, Fig. 17

184. This module is an optional item and only fitted to 6500 when remote facilities are required. The module when connected to the rear panel, allows direct connection from a GPIB talker/listener device and implements the full IEEE 488 specifications (no control function).

185. IC1(8291) GPIB talker/listener integrated circuit is connected to the microprocessor system providing both talker and listener capabilities. IC2-IC5 transceivers are used to translate the negative true logic and act as drivers. IC6d/IC6c provides the logic 'low' level for the receive instruction T/R1 to IC4, pins 7,9; or the talker 'high' level for IC2,IC3,IC4 and also provides the additional buffering necessary for the three ICs in line. Also fitted on the interface module are the GPIB bus terminator loads R1-R6, the address switch SW1. and its buffer IC7.

186. The function of the board is to provide buffering between the general purpose interface bus and the 8291 GPIB handler. The external controller directs the flow of data on the bus and designates when the 6500 is to send data and when it must receive it. The bus uses 16 signal lines to connect all units of a system in parallel. These lines are sub-divided into data, transfer and interface management buses as shown in Fig. 18.

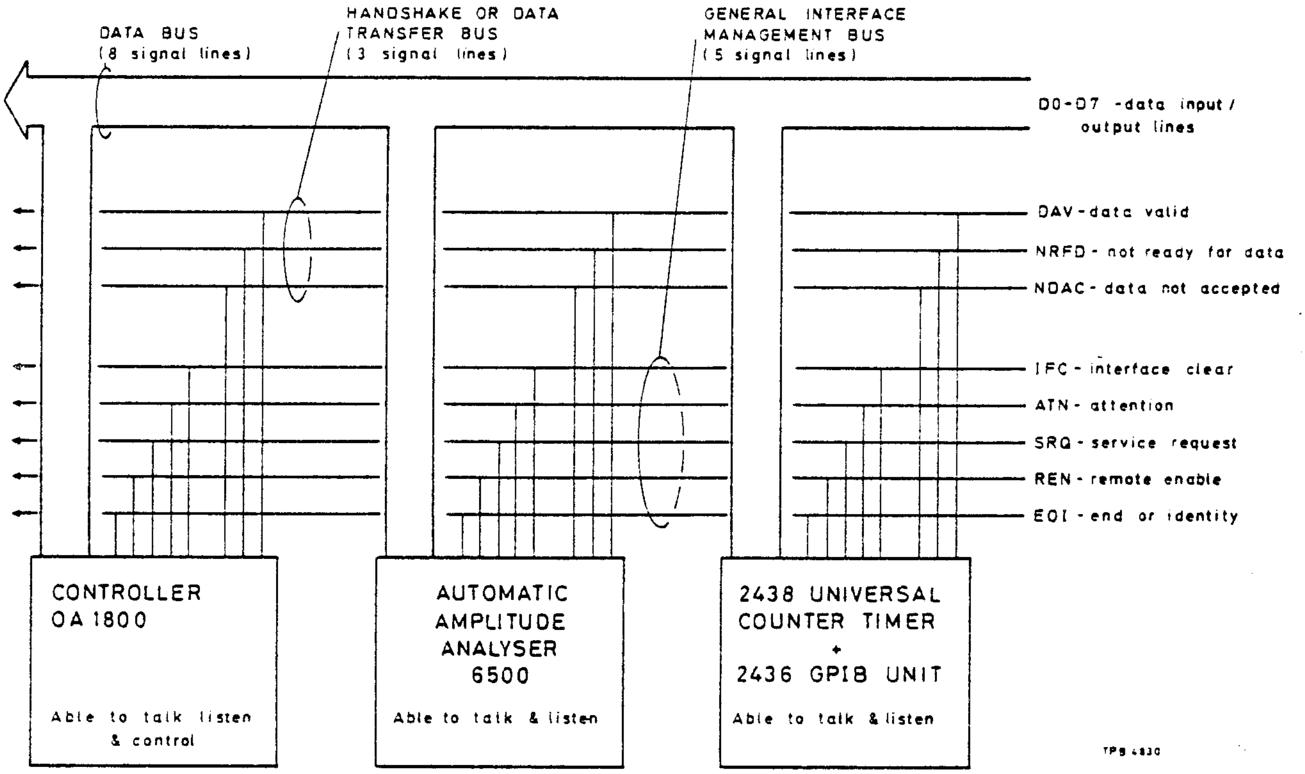


Fig. 18 Interface bus structure

187. Data bus, comprises 8 data input/output lines D0-D7 and is used to transfer the data (commands, addresses and instructions) in bit parallel, byte serial form.

188. Interface management bus, manages the orderly flow of data across the interface and consists of 5 wires carrying the following signals:

Interface clear (IFC); sent by the system controller to clear all device interfaces so that they set to an initial condition.

Remote enable (REN); sent by the controller to enable instruments to be placed under remote control.

Attention (ATN); sent by the controller to indicate that an address or command is on the data lines.

End or identify (EOI); an instrument or controller signal sent to indicate the end of a message.

Service request (SRQ); sent to a controller by an instrument to indicate that it needs service. This can be programmed using the 'SQ' program code, details of which are given in the Operating Manual, Vol. 1, Chap. 3-1 SRQ (Service Request) Functions.

189. Handshake or data transfer bus, co-ordinates the flow of data and comprises 3 lines which are used for the handshaking process, by which a talker or controller synchronizes its readiness to send data with a listener's readiness to receive data. The handshake signals are:

Not ready for data (NRFD); asserted (low) by a listener when it is active and not yet ready to receive data. Set high to signal its readiness to receive data, DAV can then be signalled if further data is to be processed.

Data valid (DAV); asserted by a talker to indicate that the data it has placed on the data bus has settled and may be accepted.

Not data accepted (NDAC); asserted by a listener when receiving information from the data lines. Release of the NDAC line tells the data source that new data can be submitted.

190. **Bus operation**

(i) A sequence of messages may be commenced by the controller asserting IFC on the management bus to set the interface to its initial condition.

(ii) The controller then sets up which instruments are to be listeners by asserting ATN and handshaking the personalized listen address of these instruments over the bus. Similarly the controller designates the talker (only one instrument may talk at a time) by sending its talk address, again with an ATN asserted.

(iii) On release of the ATN command (i.e. ATN) the talker is then able to place data on the data lines D0 to D7, the transfer of this is controlled by the handshake process and is received by all addressed listeners. The talker typically concludes the sequence by asserting EOI and the controller then resumes control.

(iv) Both the talker and the listeners may be switched by the controller into an inactive state by asserting IFC or sending OTA (other talk address) and UNL (unlisten) on the data bus.

191. Handshake procedure, the handshake is used whenever data is transferred on the bus. When a signal is asserted the function indicated by the line is carried out, e.g. NRFD is asserted to signify the listener's unreadiness to receive data, and unasserted or removed when ready to receive data. A typical handshake is as follows:

(i) Talker (controller) places a byte on the data bus with DAV initially unasserted to show data is not yet valid.

(ii) When all listeners are ready to receive data NRFD is removed with NDAC at this time asserted.

(iii) After a delay to allow the data bus to settle, talker asserts DAV to show data is valid and may be accepted.

(iv) Data byte is transferred, then listeners assert NRFD. When all the listeners have accepted the byte NDAC is removed to signify receipt.

(v) Talker removes DAV, listeners assert NDAC, and the bus reverts to its initial condition ready for the next data byte, a typical cycle is shown below in Fig. 19.

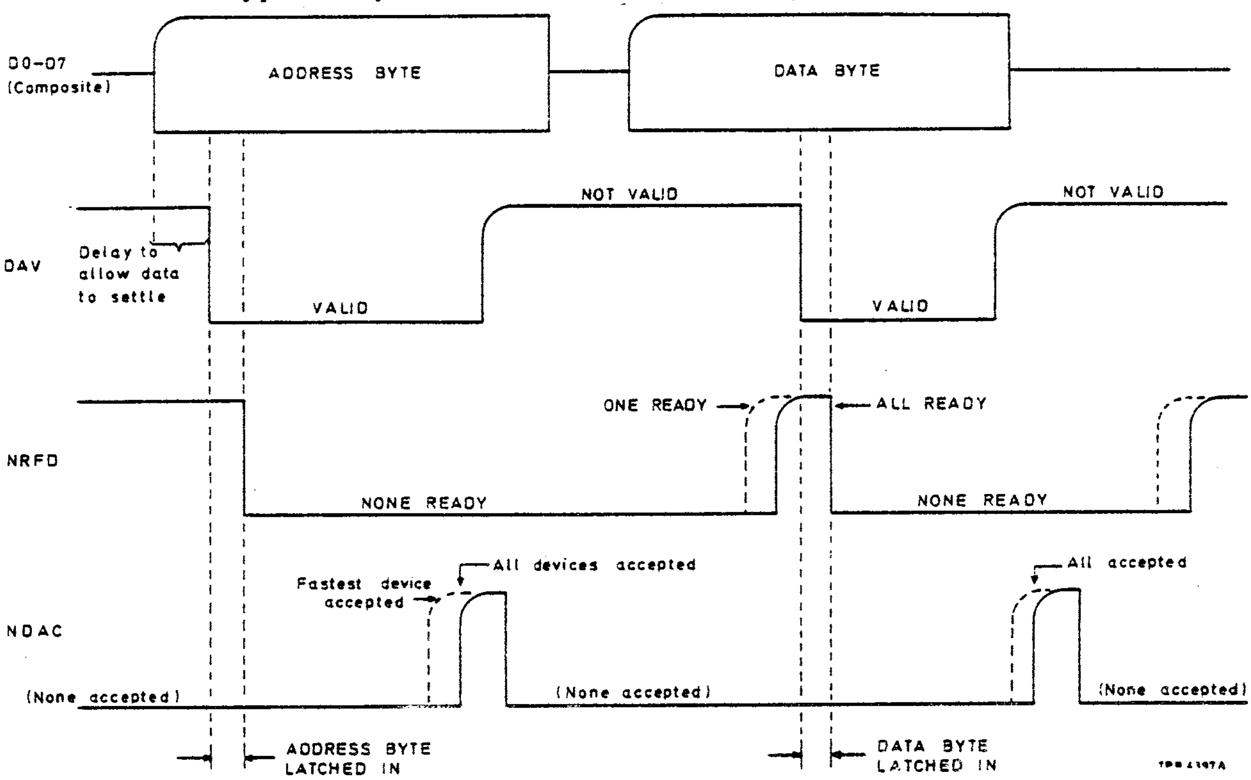


Fig. 19 Handshake procedure

Chapter 5

MAINTENANCE

CONTENTS

INTRODUCTION

1. This chapter contains information for keeping the equipment in good working order, checking overall performance, fault finding and realignment procedures. Before attempting any maintenance on the equipment you are advised to read the preceding chapter containing the technical description.

2. Test procedures described in this chapter may be simplified and of restricted range compared with those that relate to the generally more comprehensive factory test facilities, which are necessary to demonstrate complete compliance with the specifications.

3. Performance limits quoted are for guidance and should not be taken as guaranteed performance specifications unless they are also quoted in the performance data in Chap. 1. When making tests to verify that the instrument meets the stated performance limits, allowance must always be made for the uncertainty of the test equipment used.

4. In case of difficulties which cannot be resolved with the aid of this book, please contact Marconi Instruments Ltd., Microwave Products Division, or your nearest Marconi Instruments representative. Always quote the type and serial number found on the data plate at the rear of the instrument.

5. Integrated circuit and semiconductor devices are used throughout this instrument and, although these have inherent long term reliability and mechanical ruggedness, they are susceptible to damage by overloading, reverse polarity and excessive heat or radiation and the use of insulation testers.

Static sensitive devices ⚠

6. The c.m.o.s. integrated circuits used in this instrument have extremely high input resistance and can be damaged by accumulation of static charges (see preliminary pages, Notes and Cautions). Boards that have such integrated circuits all carry warning notices against damage by static discharge. Care must also be taken when using freezer sprays to aid fault finding. These can create a static charge likely to change the programmed memory of (E)PROMS.

Safety in the handling and disposal of cathode ray tubes ⚠

7. The risk of implosion of cathode ray tubes although not high, is a real one and in the event of it occurring, severe injuries may be inflicted - heavy pieces of glass moving at high velocity can cut and maim. In order that risk of implosion is reduced to the minimum the following code of practice must be observed in those places where c.r.t's are handled and used.

8. **Handling.** All personnel must be advised of the hazards involved in the use and handling of c.r.t's. A tube not in use should always be stored in the manufacturer's package, to prevent accidental damage, and in the event of an implosion glass fragments will thereby be contained. It is essential that when lifting or carrying tubes no undue stress is imposed upon the neck or in the area of the neck to bulb flare - never carry or turn a tube over by grasping the neck. Where practical, handling and installation of tubes should be carried out in a screened or separate section, thereby reducing the risk to personnel who are in the vicinity but not involved in the operation.

9. A tube with a scratched or grazed face plate is a potential hazard as any residual mechanical strains present in the glass migrate towards the scratch and link up.

10. When standing a tube on its face, ensure that it rests on a clean surface, free from grit and hard particles likely to cause scratching. A studded rubber car mat provides an excellent surface. A tube's strength can deteriorate with age therefore do not fit or remove the same unnecessarily.

11. Protective clothing should be provided i.e. Heavy weight face screen (BS 2092), Safety spectacles, Chrome leather bib style apron, Mordant leather gauntlet gloves with 150 mm (6") cuffs and Chrome leather oversleeves. The clothing should be stored in a suitable cupboard and the contents itemised if practical. Supervisors should ensure that the protective clothing is worn.

12. **In the event of an accidental implosion.** Personnel cleaning up broken tubes must do so with care, avoiding possibility of contamination of cuts with the coating materials and hands must be thoroughly washed after removing dust from clothing etc., to prevent accidental injestion of chemicals which may be harmful. Because of the possible risk of broken fragments of glass and contamination of the leather with the phosphor coating of the tube it is essential that sleeves, gloves and apron are carefully cleaned and if necessary - disposed of, after being used in connection with a breakage.

13. **Disposal of scrap cathode ray tubes,** it is important that all personnel are made aware of the hazard of placing tubes, with a good vacuum, into normal waste disposal. The danger is a real one if the tube should implode while being moved or handled. To prevent such an incident it is advised that tubes

be completely smashed before disposal. This task must only be undertaken by competent personnel and no attempt should ever be made to smash a tube or destroy a vacuum without taking adequate precautions to prevent the glass from flying.

14. When destroying a tube, a convenient method of preventing glass scattering can generally be devised by adapting the carton in which the replacement tube was supplied, together with its die-cuts and moulded inserts. The tube should be placed face downwards in the bottom of the carton and the die-cuts and moulds positioned above the bulb and around the neck so as to contain the collapsing glassware. A short section of the tube neck at the base end should be left clear of the protective material sufficient to allow it to be struck with a ballpein hammer used at arm's length, in a hand protected with a leather glove. This operation can generally be accomplished with the hand just inside the carton, the lid of which is used as an extra precaution against the possibility of small glass particles flying upwards from the neck. It is also a wise precaution to leave the lid on the carton for a short time after the glass has shattered to allow the dust to settle, thus preventing the possibility of inhaling it.

15. If the original carton is not available a strong cardboard carton or wooden box can be used just as effectively to contain the flying glass, provided heavy sacking or similar material is used around and above the bulb to prevent the glass flying upwards. It is essential that a round object such as a ballpein hammer be used, tools with sharp corners or points must be avoided. It is also important that the tube should not be struck anywhere but at the neck close to the base pins.

16. The smashed tubes may be disposed of in the same manner as one would dispose of any broken glass and it is advisable to label the carton as containing

'GLASS - BROKEN CATHODE RAY TUBE'

Fault location

17. Some aid to fault finding is provided by the typical d.c. voltage and signal levels. Tables given are not extensive but are intended as a pointer to further investigation. It is emphasized that each fault table should be studied having regard for the others, since incorrect operation of a circuit may be caused by malfunction of an associated circuit.

DC voltages

18. Voltages given approximate those which can be expected using a 20 kΩ/V meter on a typical 6500 connected to an a.c. supply of 220 - 240 V, 50 Hz.

Air cooling

19. Cooling of this instrument is effected by drawing cooling air through the instrument's lower cover via two slotted entries, each one is covered by a strip of polyurethene foam. The fan unit is mounted on the power supply unit

chassis with the output ducted through another filter mounted in the centre of the rear panel. The fan requires no maintenance but the filters should be cleaned periodically

(a) Withdraw the detachable filter, first removing the cover from the rear panel. Clean all filters and the cover with a suction cleaner and, if necessary, wash with hot soapy water. Under no circumstances should solvents be used.

(b) Shake the filters dry, if necessary, and replace.

Board layout and preset components

20. Printed circuit board component layouts can be seen in Chap. 7, Servicing Diagrams. Preset and select-in-calibration (SIC) components are also identified there. A further plan view of the presets and their function can be seen in this chapter. Edge connector destinations are also shown in Chap. 7, these have two rows designated 'A' and 'B'. Row B is nearer to the c.r.t. assembly. Edge connector pins are numbered 1 to 32 with pin 1 nearest to the front panel. Boards must be inserted with components side nearest to the c.r.t. assembly.

ACCESS AND LAYOUT

Layout, top view, see Fig. 1

21. To remove top and bottom outer covers simply unscrew the two retaining screws situated on the rear panel; slide each cover to the rear and lift off. Access to the boards AC01 - AC12 can be obtained by unscrewing the clamp card retainer screws until the slides inserted in side and centre frame can be withdrawn and the retainer removed.

22. An extender board (offered as an Optional accessory) may be used to place the boards into the servicing position as shown in Fig. 1. Some boards will not operate correctly in such a position. Further information on this is given in the calibration procedures.

23. CRT Access ⚠ Direct access to the c.r.t. is restricted as a safety measure and only competent personnel who are familiar with the hazards involved should lift the tray covering the c.r.t. unit. The tray is secured with six screws, three of which are accessible on the outside of the left-hand side panel and three on the centre support frame. Remove the four screws nearest to the front of the instrument and slacken the two rear screws to allow the tray to pivot into the vertical plane, re-secure these again to maintain the servicing position.

WARNING ... ⚠

When lifting the tray ensure that movement of the cableform is not impeded by the neck of the c.r.t. or its associated AT02 which is positioned around the neck of the tube.

24. Before servicing also read the paragraphs in this chapter relating to Safety in the handling and disposal of cathode ray tubes and c.r.t. fitting and display setup, safety precautions.

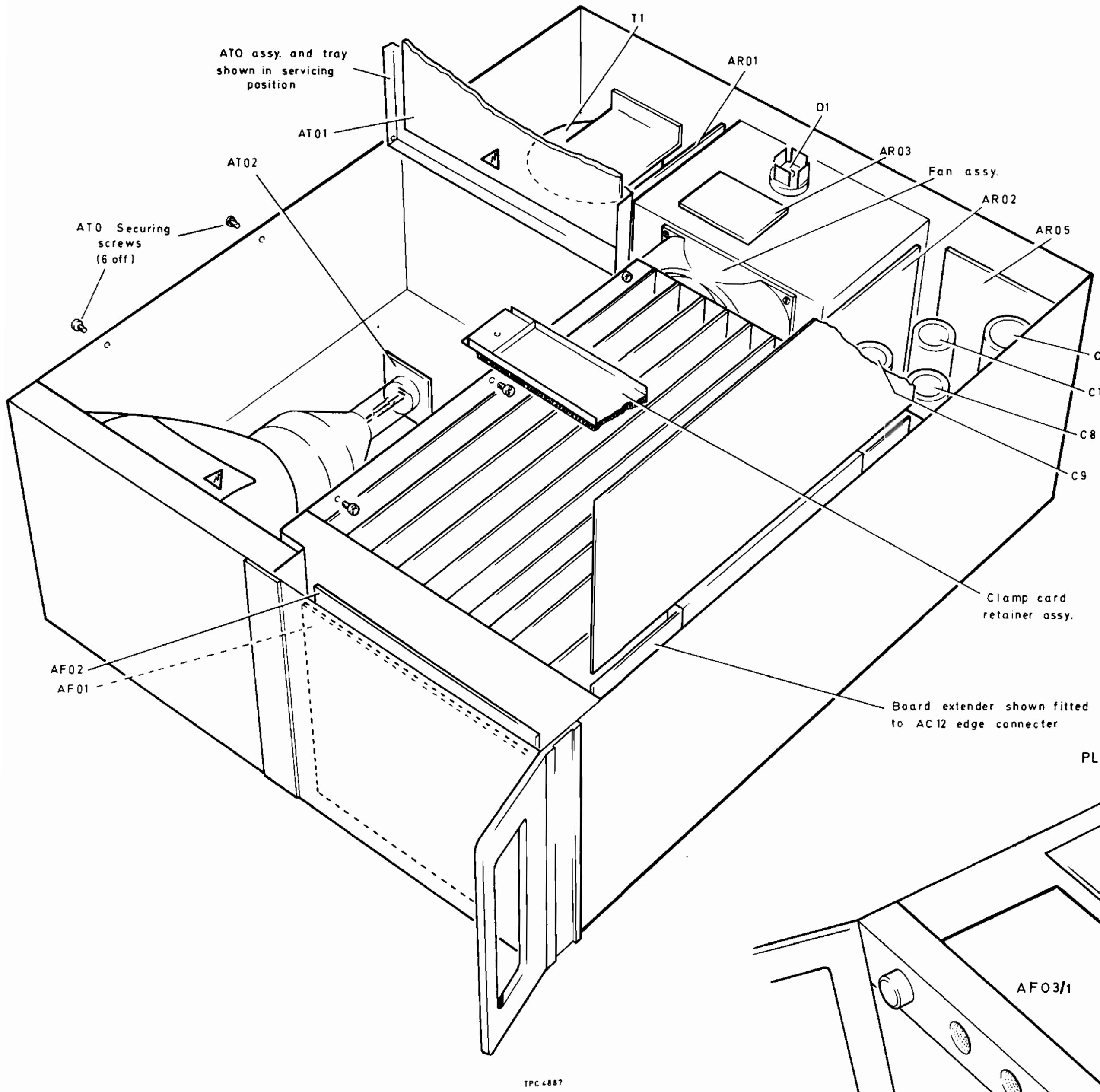


Fig. 1 Layout, top view.

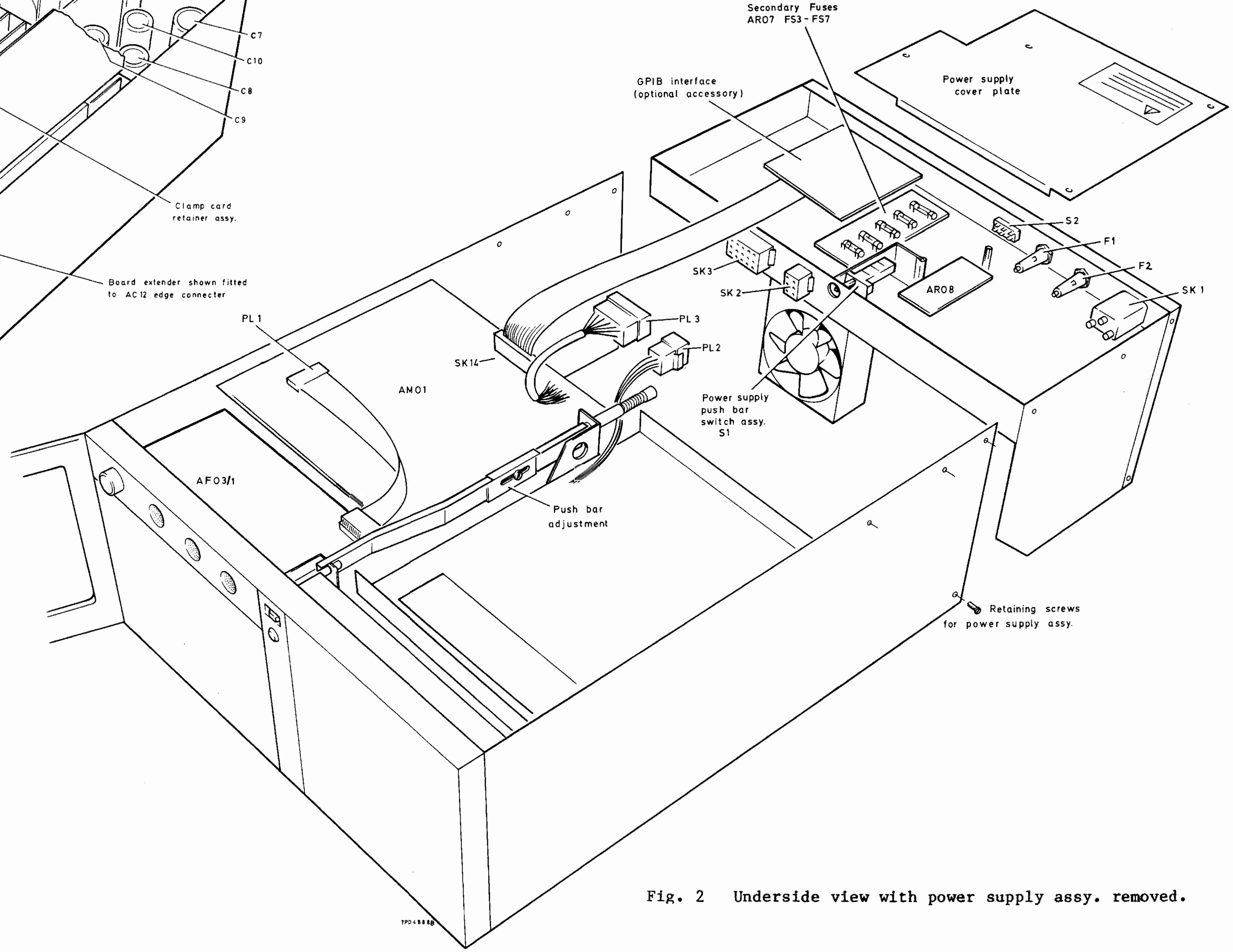


Fig. 2 Underside view with power supply assy. removed.

Underside view, see Fig. 2

25. Secondary fuses on board AR07 are all low voltage and so are all readily accessible, if however access is required in the high voltage area it is essential that the supply voltage is first disconnected from the instrument. Only then should the power supply cover plate be removed to reveal board AR08, SK1, SK2, fuses F1 and F2, and the push bar switch S1.

26. Access to board AF03/1 can be obtained by first disconnecting the molex connector SK1 and the conhex r.f. connector, remove the four securing screws on the top of the cover plate and this can then be removed.

Removal of power supply assy.

27. In normal circumstances it should not be necessary to remove this except in the event of either fan motor renewal or major servicing, however if required carry out the following procedure :-

(1) First detach the rear end of the side carrying handles by first prizing off the plastic cover to disclose the end cap and handle securing screws. Unscrew the handle screw followed by the end cap screw to release the rear side handle fixing. Now remove the eight power supply assy. retaining screws shown in Fig. 2.

(2) Disconnect AC09/2, PL1, PL2, and PL3; if the optional GPIB interface is fitted also disconnect SK14. Carefully pull the power supply assy. to the rear taking care not to distort the push bar or switch S1 when separating the unit.

(3) On replacement it may be necessary to mechanically re-adjust the push bar to operate the switch S1 correctly. This is easily done by slackening the retaining screw in the distance piece situated in the centre of the push bar then altering the effective length as necessary before re-securing the screw.

Removal of AF01/AF02 assy.

28. First remove the right-hand side front handle trim infill and handle as shown in Fig. 3b. Then remove the front trim infill followed by the trim strip held by four screws. Four further screws, two on the top and two on the bottom secure the assy. The two bottom screws can be easily accessed using a long handled screwdriver. A mounting plate is also used to position the assy. correctly, this is placed on top of the assy's. bottom flange.

29. To avoid possible damage on AF02 board ensure that PL2 is disconnected before attempting to lift out the assy. It may also be necessary to remove some of the buttons from keyboard AF01 to enable sufficient clearance to pull the assy. clear of the front panel. These can easily be removed by pulling firmly on the button. Finally disconnect AF02, PL1 and withdraw the assy.

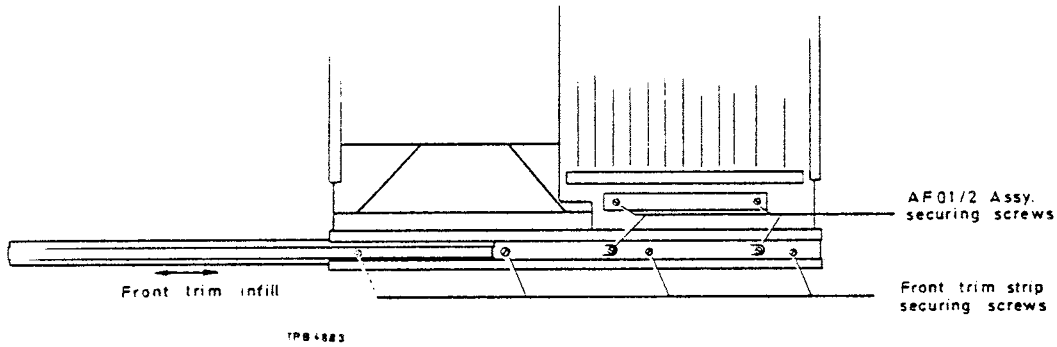


Fig. 3a Front trim strip and AF01/2 assy. securing screws.

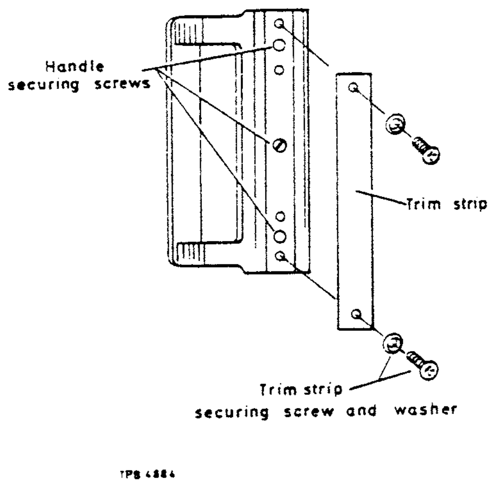


Fig. 3b Handle assy.

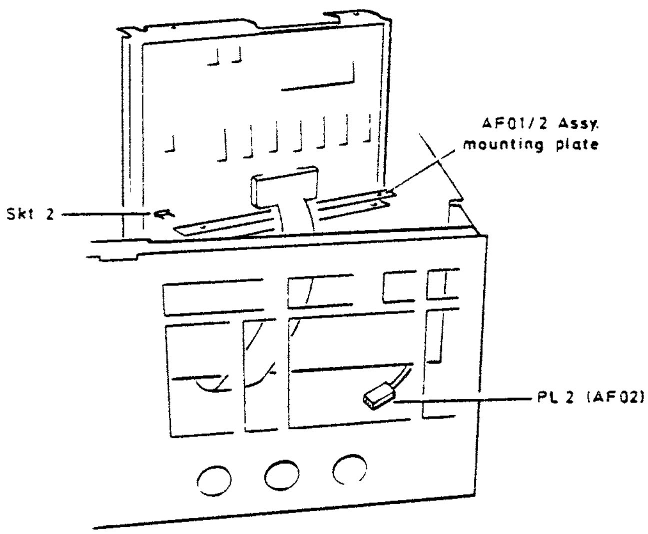


Fig. 3c AF01/AF02 assy. removal.

Fig. 3 AF01/AF02 assy. removal

PERFORMANCE CHECKS

Overall tests and adjustments

30. Many of the tests described in this chapter are simplified and of restricted range compared with those which would demonstrate compliance with the specification as described in paras. 1 to 4. If the results quoted in the following paragraphs are not obtainable refer to the related fault finding and re-calibration sections.

31. Check that the correct mains supply voltage is applied and that the correct fuses are fitted, for details see Operating Manual. To prevent damage to the c.r.t. coating initially turn the intensity control to minimum then select SUPPLY ON. The microprocessor should be running, this may be checked by pressing SHIFT key which will cause SHIFT l.e.d. to toggle on/off.

32. Self test and a simulated failure can also be checked as described in the Operating Manual Chap. 3-1. Also connect the required microwave sweeper to the 6500 and terminations, connectors and cables necessary as listed in Chap. 3-1 following Fig. 2.

Functional checks

33. Connect the 6511/6512 Detectors then perform the following checks :-

Intensity controls	-	Check Intensity, Graticule Line B then Line A controls for smooth operation with no flaring of the trace.
Brightline control	-	Check smoothness of operation and correct directional sense i.e. clockwise moves brightline right and vice-versa.
Check keys	-	Ensure correct mechanical movement and the operation of all keys in the following order :-
SHIFT :	-	Check operation of l.e.d. also.
SWEEP :	-	NORMAL AVERAGE FREEZE
LOCAL :	-	Check only for mechanical operation if GPIB interface is not fitted.
MODE :	-	A, B, A & B, R, -R STORE (Cancel with NORMAL) SUB MEM (Cancel with NORMAL) UNITS.
SET :	-	DATUM RANGE START STOP

DISPLAY :	-	HIST (Line A) LINE (Line A) HIST (Line B) LINE (Line B)
PLOT		
BRIGHTLINE :	-	ΔF MAX MIN MARKER
AUTO :	-	F1 - F2
NUMERIC KEYPAD : & ENTER	-	(Use DATUM when testing numeric keys).

34. Check the correct operation of each of the signal channels by ensuring that the detector will auto zero correctly when connected to each channel in turn and gives the correct c.r.t. display.

Detector input	Display
Connect to A input, auto zero and check :-	A Ready B No probe R No probe
Connect to B input, autozero and check :-	A No probe B Ready R No probe
Connect to R input, autozero and check :-	A No probe B No probe R Ready

Note ...

The ZERO facility should only be used with no incident r.f. at the detector. When each channel has been successfully zeroed select AVERAGE, each channel should display a power level between -55 and -61 dB.

Calibration aid facility

35. The CALAID function provides a visual indication of the state of the signal channel amplifiers. When in CALAID it is possible to disable all temperature compensation in the instrument.

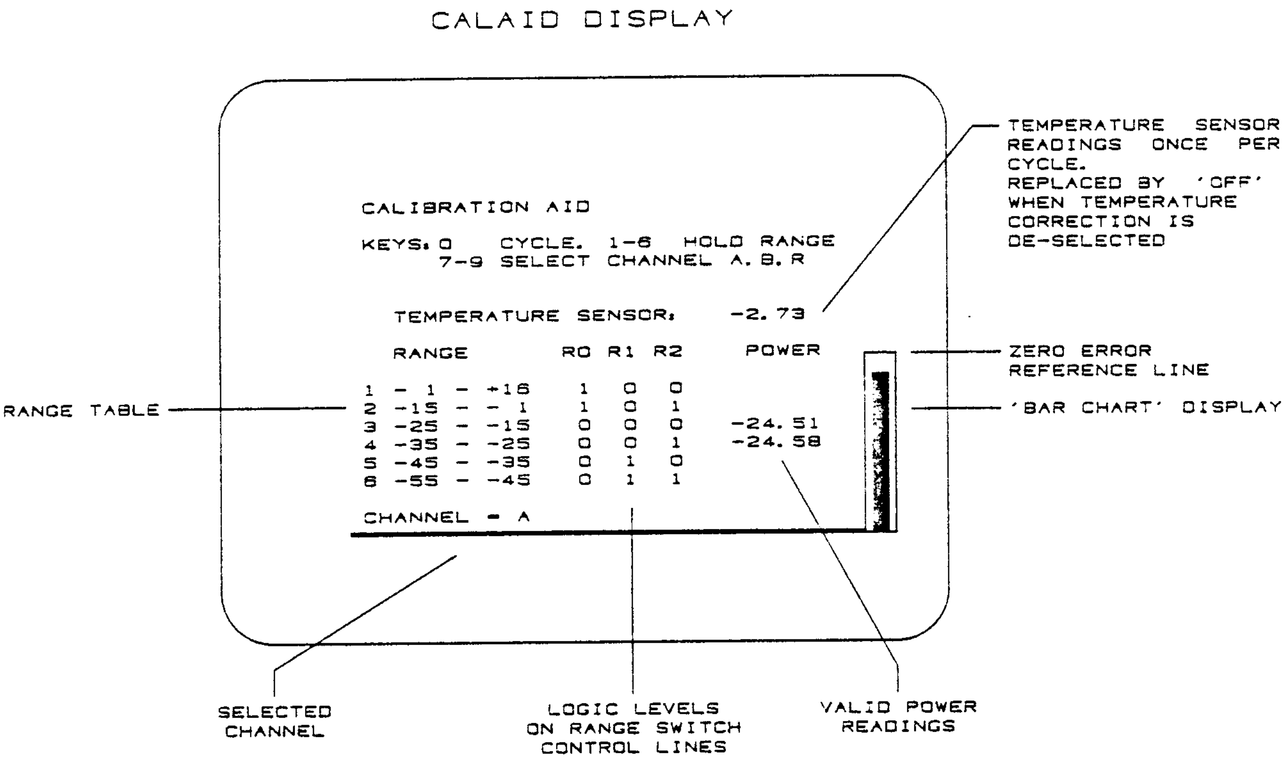


Fig. 4 CALAID display

36. The signal channel gain may be programmed in 10 dB steps giving the six ranges shown in the CALAID display. When operating in its normal CYCLE mode, CALAID programs the signal amplifier for each range in turn from 1 to 6. The average of a number of power measurements is calculated for each range. If the readings are valid; that is, the range selected provides neither too little nor excess amplification, the result (corrected for square law deviation and temperature as usual) is displayed in the POWER column on the c.r.t. If a valid reading cannot be obtained for the range, a field of blank characters is written to the screen.

37. Because the ranges overlap by approximately 1 dB, it is possible to obtain valid readings on two ranges simultaneously. The instrument is calibrated to ensure that the same reading is obtained on both ranges in the overlap region. The BAR-CHART display provides a graphical representation of the tracking between ranges. If two adjacent ranges give valid readings the bar chart height varies to represent the error.

38. The bar chart display is deliberately slowed by averaging to remove noise effects. The full screen height of the BAR-CHART display is 1 dB with the reference line representing 0 dB tracking error between ranges. If the bar aligns with the reference line or is within approximately 1/8" of the reference line, range to range tracking is better than 0.02 dB.

CALAID operation

39. When in CALAID - issue commands with the numeric keypad and to exit use a MODE or NORMAL key.

(1) Select Channel A with numeric key 7
Channel B with numeric key 8
Channel R with numeric key 9

(2) Select or deselect temperature compensation - Select SHIFT and SECRET keys.

(3) Select normal range cycle operation with '0' - This mode is automatically selected when CALAID facility is first initiated.

(4) Hold range 1 - 6, flashing letter H gives an indication of a held range - Range held corresponds to numeric key pressed, readings are taken repeatedly on the selected range.

Notes ...

(1) To release from a held range either press 0 to resume cycling or re-select the required channel e.g. press 7, 8 or 9.

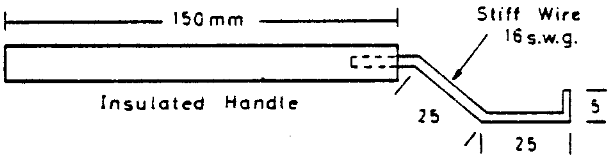
(2) The BAR CHART reference line on the screen represents zero tracking error between ranges - full screen range 1 dB.

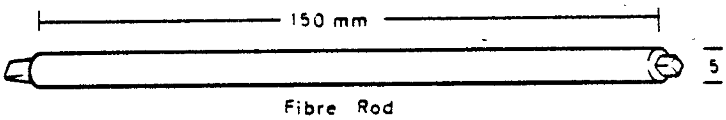
TABLE 1 TEST EQUIPMENT

Item	Description	Minimum use specification	Recommended model
a	Multimeter	Greater than 20 kΩ/V	GEC Selectest
b	Oscilloscope	Bandwidth : 50 MHz Volts/division : 5 mV to 20 V	TELEQUIPMENT D83
c	Oscilloscope probe		
d	RF power source	Variable from -50 dBm to 0 dBm	6058B
e	50 MHz 0 dBm Calibrator box	With current calibration certificate	Available in Power meters Type 6950 or 6960
f	Detector 6511 (Std)	Standard detector 6511 with calibration certificate	6511
g	Detector 6511 (General purpose)	Specification as laid down in H 6500 Vol. 1 Chap. 1	6511
h	Digital voltmeter	DC volts 0.1 V - 100 V Accuracy 0.001%	DATRON 1061 or HP 3456A

TABLE 1 TEST EQUIPMENT (continued)

Item	Description	Minimum use specification	Recommended model
i	Sweep oscillator & plug in Oscillator unit	For details of use see H6500 Vol. 1 Chap. 3-1 Preparation for Use paragraphs	MI 6700B MI 6600A/1 Series
j	Logic probe		
k	Variac		
l	Resistance box (with 6511 probe connector)		
m	Electro-static voltmeter	Voltage range 0-15 kV	
	Special Tools and alignment aids		
n	Card extender	Used to elevate boards AC01-AC12 into a servicing position	MI(Microwave products) 3964-268
o	IC Test clips	16 pin dual-in-line (2 off)	-
p	Alignment graticule	As per dwg. number 2200/346 Issue 1	MI(Microwave products)
q	Pot/shift ring adjuster		
r	Width/Linearity core adjuster		





ADJUSTMENT AND CALIBRATION

Voltage checks ⚠

Test equipment : items h, Digital voltmeter
k, Variac
b,c, Oscilloscope & probe

40. 210-250 V (50 -60 Hz) Range setting. Ensure that the mains input (voltage selector on the rear panel is set for the above range and that the correct fuses are fitted in F1 and F2 (600 mA time delay). Connect the 6500 input supply voltage via a variac set to give a voltage output of 230 V a.c.

(1) Switch on a.c. supply, check that fan unit is running.

(2) Locate the power supply output tags on AM01 Motherboard and check that each of the following stabilized d.c. voltages is within the limits shown in Table 2. Check also that the maximum ripple level is not exceeded.

(3) Reduce the variac voltage to give an output of 210 V a.c. and check again that the limits shown in Table 2 are not exceeded. Raise the variac voltage to give an output of 250 V and once more check that Table 2 limits are not exceeded.

TABLE 2 DC VOLTAGES

Range	Output Voltage		Max ripple	Connections
	Min	Max	Level	
+5 V (OVD)	4.75 V	5.25 V	7 mV	AM01 (Motherboard)
+24 V (OVD)	22.8 V	25.20 V	10 mV	tag positions
+15 V (OVD)	14.25 V	15.75 V	5 mV	are identified
-15 V (OVD)	14.25 V	15.75 V	5 mV	in Chap. 7 Fig. 18a
+15 V (OVA)	14.25 V	15.75 V	5 mV	AM01 printed circuit
-15 V (OVA)	14.25 V	15.75 V	5 mV	connections.
+12 V	11.10 V	12.90 V	10 mV	Board AR03 pin 7.

41. <u>105-120 V (50-60 Hz) Range setting.</u> Ensure that the mains input (voltage selector) on the rear panel is set for the above range and that the correct fuses are fitted in F1 and F2 (1.25 A time delay). Connect the 6500 input supply voltage via a variac set to give a voltage output of 115 V a.c. then carry out the checks detailed in the previous paragraph steps 1 to 3 except that in step 3 variac voltages set should be lowered and raised to 105 V and 120 V respectively, limits given in Table 2 are unchanged.

CRT alignment (AT01/1,AT02) ⚠

Test equipment: items a, Multimeter
p, Alignment graticule
q, Pot/shift ring adjuster
r, Width/linearity core adjuster

42. If a replacement c.r.t. is to be fitted, instructions on procedure and precautions to be taken whilst doing so are given in the Fault location and Repair section of this chapter. Note that because the c.r.t. is scanned vertically in 6500 the FRAME controls affect the horizontal picture characteristics and the LINE controls affect the vertical characteristics.

43. Remove the left hand side front handle and slide the alignment graticule into the filter slot on the front panel observing the correct orientation. Centre all controls on AT01/1. Turn the front panel INTENSITY control fully clockwise. Remove all correction magnets from the yoke if fitted and ensure that the yoke fits snugly against the c.r.t. bulb.

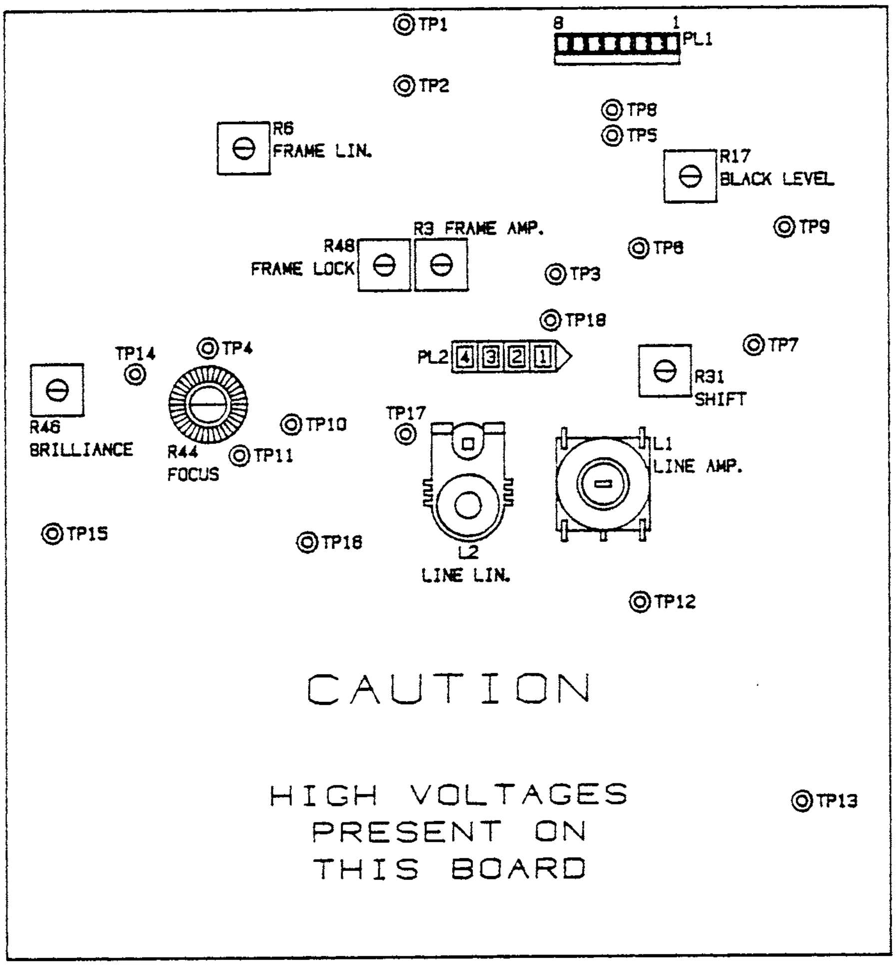


Fig. 5 AT01/1 Calibration component chart

⚠ WARNING LIVE PARTS ⚠

44. The c.r.t. electronics employs high voltages. Use only the special test equipment items when making adjustments within the c.r.t compartment. Avoid touching any wire links or test points on AT01/1,AT02, scan coil connections. It is advisable to avoid placing more than one hand into the compartment. Keep the other hand in the pocket to avoid touching earthed surfaces.

45. Switch on the 6500, a test pattern will be generated during the power-on self test. To maintain the test pattern hold down any key. Wait until the front panel l.e.d's flash before releasing the key. The test pattern can also be generated without switching off the instrument simply by short circuiting the reset pads situated on board AC18 while holding down a key. These can be identified by reference to Chap. 7, Fig. 5a Component layout diagram.

46. Allow 30 minute's warm-up time before commencing the realignment then proceed with the alignment of board AT01/1 as follows:-

(1) Set multimeter to d.c. V, 100 V full-scale. Connect the negative lead to TP2 and the positive lead to TP9. Adjust R17 (BLACK LEVEL) to obtain a reading of 70 V ±1 V. Note that the high frequency response of the video amplifier is reduced by the impedance of the multimeter, but this does not affect the d.c. measurement being made.

Remove the multimeter probes and adjust R46 (BRILLIANCE) to give a visible display.

(2) Adjust R48 (FRAME LOCK) to give a synchronized display. When a stabilized display is obtained, re-adjust R48 to a point halfway between the setting at which a stabilized display is obtained and the end of the potentiometer's travel or the point at which synchronization is again lost.

(3) Re-adjust R46 (BRILLIANCE) to obtain a visible background raster. Adjust front panel INTENSITY to give the clearest possible display.

47. Line adjustment

(1) Adjust R31 (SHIFT) to centralize test pattern with respect to the displayed raster.

(2) Adjust L1 (LINE AMPLITUDE) for correct picture height.

(3) Rotate L2 (LINE LINEARITY) inductor magnet to obtain optimum linearity using the vertical linearity lines on the test pattern as a guide.

(4) Re-adjust L1 (LINE AMPLITUDE) if necessary.

48. Frame adjustment

(1) Adjust R3 (FRAME AMPLITUDE) for correct picture width.

(2) Adjust R6 (FRAME LINEARITY) for optimum linearity using the horizontal linearity lines on the test pattern as a guide.

(3) Re-adjust R3 (FRAME AMPLITUDE) if necessary.

49. Picture centring. Centre the display by rotating the Shift rings on the deflection yoke assembly. Use the central cross on the test pattern and the centre marking on the test graticule as a guide.

Note ...

Adjustments to L1,L2,L3 and R6 are interactive - repeat these if required.

50. Picture shape adjustment. If necessary rotate the scan coil assembly to square the c.r.t. picture. Correction magnets may now be mounted on spigots on the deflection yoke. Adjust the correction magnets to obtain the best possible picture shape. Ensure that the outside edge of the test pattern is square, and fits within the two scribed lines of the test graticule.

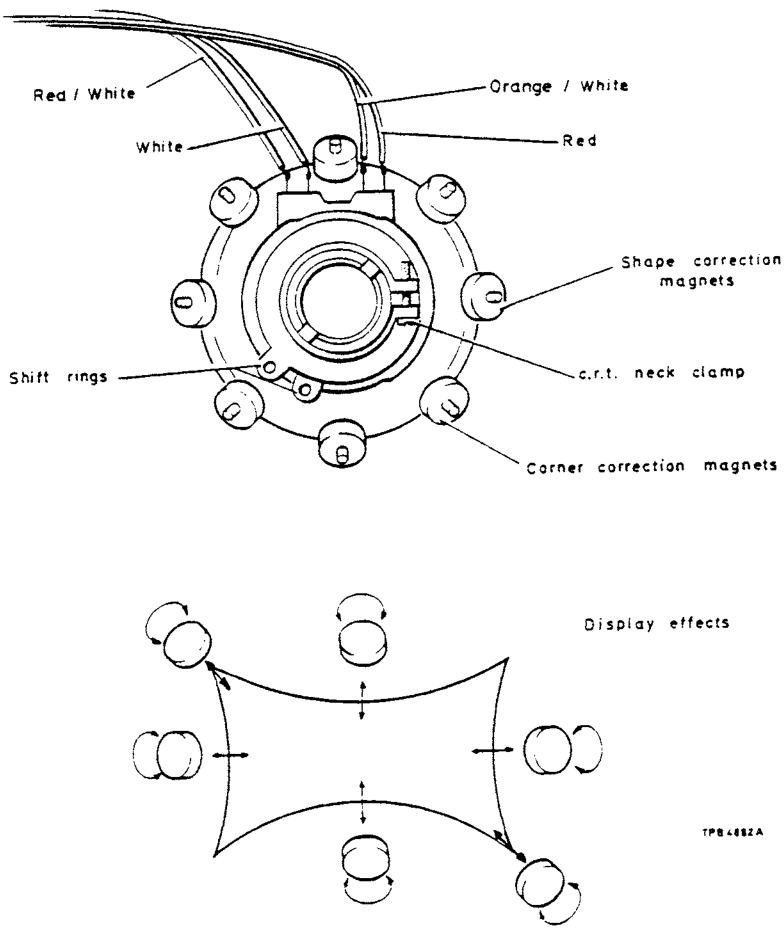


Fig. 6 CRT coil assy. adjustments

51. Straighten top and bottom edges and vertical sides using rotateable magnets corresponding to those positions. More than one magnet may be placed on a spigot if required. Add corner correction magnets if required.

Note ...

Adjustments made previously to L1,L2,R3 and R6 are interactive - repeat these if required.

52. Reduce brightness using R46 (BRILLIANCE) control until blank raster areas just disappear. It is important to note that the correct operation of the video mixer depends on this adjustment. With the front panel INTENSITY control adjusted for the clearest display, adjust R44 (FOCUS) for optimum focus. This can best be achieved by focusing on alphanumeric characters e.g. the 'SELF TEST' message.

53. Finally fix the coil assembly, magnets and shift rings using a suitable adhesive such as 'Silastic 732 silicone adhesive/sealant'. Take great care not to disturb the picture shape magnet and carry out a final check on the c.r.t's alignment before allowing the adhesive to set.

Spinwheel circuit adjustment (AF02)

54. The purpose of this adjustment is to ensure the displayed 'Brightline' does not drift due to spurious pulses generated by the 'Spinwheel' circuit on AF02. Carry out the following procedure :-

(1) Adjust AF02 (R27) to mid travel. Switch on the 6500, and await the display.

(2) Attempt to centre brightline using the front panel rotary control.

Note ...

The brightline may drift to right or left.

(3) Rotating R27 anticlockwise from the mid-position eventually causes the brightline to drift left, and similarly rotating R27 clockwise causes brightline to drift right. Adjust therefore R27 to minimize drift in either direction. After this ensure that clockwise rotation of the front panel rotary control moves the brightline smoothly to the right, and anticlockwise, to the left.

Video mixer adjustment (AC04/1)

55. Display quality of the video mixer is set up in manufacture and only small adjustments should be required to improve the display. Switch on 6500 and allow 10 minutes before attempting any adjustments. Confirm that the raster is NOT visible on blank area of the display. If it is visible it will be necessary to re-adjust AT01/1 Brightness control R46, see Picture shape adjustment paragraphs.

AC01/R6 FRAME SYNC. PULSE WIDTH
AC01/R8 INTERLACE
AC01/R11 LINE DOT CLOCK

AC02/R1 LINE A DE-GLITCH
AC02/R3 LINE A DE-GLITCH

AC03/R1 LINE B DE-GLITCH
AC03/R3 LINE B DE-GLITCH

AC04/1,R5 LINE A VIDEO
AC04/1,R6 LINE B VIDEO
AC04/1,R7 BRIGHTLINE VIDEO
AC04/1,R8 GRATICULE VIDEO
AC04/1,R9 MARKER VIDEO <NOT USED>
AC04/1,R10 ALPHA VIDEO

AC09/2,R9 PLOTTER Y VOLTAGE GAIN
AC09/2,R12 RAMP/AUTO-ZERO REFERENCE

AC12/R5 STAGE 2 AMPLIFIER GAIN
AC12/R14 STAGE 3 AMPLIFIER GAIN
AC12/R33 SIGNAL OUTPUT LEVEL

AF02/R27 SPINWHEEL STABILITY

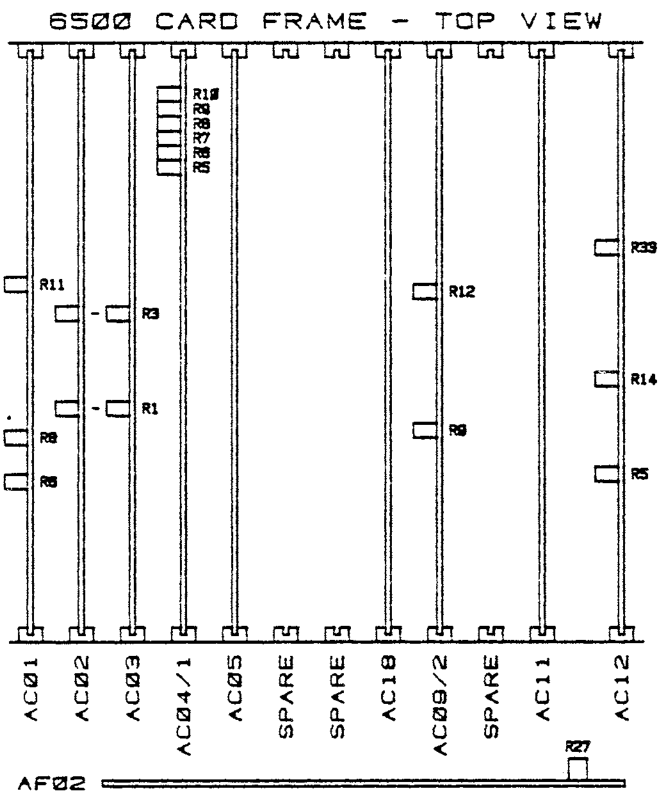


Fig. 7 Preset potentiometer adjustment chart

56. Set Graticule, Line A and Line B intensity controls to maximum and make adjustments as necessary to any of the display components following. The intensity of any component may be increased by rotating the corresponding potentiometer anticlockwise

Adjustment		Order of brightness
Alphanumerics	R10	1 (Brightest)
Line A	R5	3
Line B	R6	3
Brightline	R7	2
Graticule	R8	4 (least bright)
Small marker pips	R9 (Not used)	

Note ...

After adjustment has been made to the above controls check that with all front panel controls at minimum (except INTENSITY) all the above components are displayed. Maximum INTENSITY will result in slight smudging of alphanumerics i.e. alpha is the brightest component of the display.

Line display clock oscillator adjustment (AC01)

57. Switch on the instrument and allow 15 minutes warm-up. Adjust the front panel intensity controls to obtain a clear display of the Line A trace. The line display clock oscillator determines the vertical position of the A and B traces on the display. If the oscillator adjustment is incorrect, the position of A and B trace against the vertical scale will not match the brightline reading. In certain cases, when displaying in 'HISTOGRAM' mode the trace may 'wrap around' from top to bottom of the graticule area - giving the appearance of two traces.

58. Select a line display on memory A selecting SHIFT and MEM A. Note that at switch-on the memories are initialized to zero. Display the trace as a line - Datum 0.5 dB(m), Range 0.1 dB/Division by selecting LINE and AUTO. Then adjust AC01,R11 until the trace aligns with the horizontal graticule line corresponding to 0 dB.

Interlace adjustment (AC01)

Test equipment : items b,c, Oscilloscope & probe
n, Card extender
o, IC test clip

59. Place AC01 (Timing circuit) on the card extender, connect the test clip to IC11, switch on the instrument and allow 15 minutes warm-up. Adjust the front panel intensity controls for a clear display of alphanumeric characters. The c.r.t. display is interlaced i.e. alternate scanned frames occupy slightly different positions on the c.r.t. This adjustment sets up an interlaced display.

60. Set the oscilloscope controls as follows : Sensitivity 2 V/div., Time base 10 μs/div., Trigger slope -ve and connect oscilloscope probe to IC11 pin 7. Rotate AC01,R8 fully clockwise and note that the display is no longer interlaced (alternate scanned frames overlap and the alphanumeric characters appear to consist of discrete dots). Rotate R8 anticlockwise until the negative-going pulse length is 48 μs ±1 μs. Observe that the display is now interlaced i.e. dots forming the alphanumeric characters merge together.

Deglitch circuit adjustment (AC02/AC03)

Test equipment : items b,c, Oscilloscope & probe
n, Card extender
o, 16 pin dual-in-line IC test clip

61. Glitches occur on the line display if the microprocessor accesses the line display memory at the same time as the line generator circuit. If this is suspected it is possible to distinguish the glitches from the signal channel by selecting FREEZE. When in this mode there is no line memory update so no glitches can occur. However, signal channel noise present at the time of pressing FREEZE will remain on the display.

62. Elimination of glitches is carried out as follows :-

(1) Place AC02 (Line A display generator) on the card extender. Connect the test clip to IC5 and switch on the instrument. Allow 15 minutes warm up and select the following keys, Channel A, SHIFT, SPEED, 0 (70 ms sweep speed).

(2) Set the oscilloscope to 2 V/division Sensitivity, 1 μs/division Time base and Trigger slope to -ve.

(3) Adjust R1 to give a negative-going pulse of 5 μs at IC5 pin 4.

(4) Adjust R3 to give a negative-going pulse between 1 and 2 μs at IC5 pin 2.

Note ...

Pulses at IC5 pin 12 occur only when there is a conflict between line generator and processor memory access. This depends on the sweep timing which varies slightly according to the range and datum selected as well as the value of the measured data. With no probes connected and a consequent measured level of approximately -60 dBm, a range of 0.1 dBm/ division (obtained by selecting AUTO) will give a signal which may be displayed satisfactorily on the oscilloscope. Some adjustment of the oscilloscope controls may be required to obtain a usable trace.

(5) Confirm that no glitches are now visible on the trace. Repeat the procedure for AC03 selecting Channel B.

Plotter and Ramps adjustment (AC09/2, AR04/1)

Test equipment : item k, Digital voltmeter

63. Switch on, allow 15 minutes for warm-up. Connect the d.v.m. via a BNC connector to the RAMP (fixed 0 - 10 V) output on the rear panel.

(1) Switch the ramp output to 10 V selecting SHIFT and F2 - adjust AC09/2, R12 for 10 V ±10 mV.

(2) With the ramp output set to 10 V connect the d.v.m. to PLOTTER X output and confirm that no voltage is present - i.e. AC09/2, RL1 is open circuit.

(3) Connect the d.v.m. to PLOTTER Y output, select 'NORMAL' key to clear any messages then select 'PLOT' select option 1 'Set pen bottom left' and confirm that PLOTTER Y output voltage is now 0 V ±100 mV

(4) Select option 2 'Set pen top right' and check that PLOTTER Y output voltage is now 10 V ±50 mV, if not adjust AC09/2,R9 to achieve this.

64. Connect the d.v.m. to the RAMP (Variable 0 - 20 V) rear panel socket then select SHIFT, F2, and carry out the following adjustments :-

(1) Adjust C (COARSE) and F (FINE) presets on the rear panel for 20 V ±50 mV.

(2) Select SHIFT, F1 and adjust OFFSET control on the rear panel for 0 V ±50 mV.

Repeat steps (1) and (2) to obtain optimum readings.

Signal channel alignment (AC12)

Test equipment : items b,c, Oscilloscope & probe unit
o, Two 16 pin dual-in-line IC test clips
n, Card extender

65. Place board AC12 on the card extender and fit IC test clips to IC6 and IC14. Switch on, allow 15 minutes warm-up. Connect earth lead of the oscilloscope probe to TP5 for all measurements. Set the oscilloscope trace controls as follows :-

Vertical sensitivity	-	2.0 V/division
Time/division	-	2.0 μs/division
Trigger slope	-	-ve

66. Connect the probe to IC6 pin 9 and adjust AC12,R32 to set the negative-going pulse length to 12 μs ±0.5 μs. The position of R32 is shown in Fig. 8. Connect the probe to IC6 pin 7 and adjust AC12,R31 to set the negative-going pulse length to 12 μs ±0.5 μs.

67. Connect the probe to IC14 pin 6, set the oscilloscope to positive triggering and increase the Time/division to 5.0 μs/division. Adjust AC12,R50 to set the positive-going pulse length to 45 μs ±1 μs.

68. Connect the probe to IC14 pin 9, set the oscilloscope back to negative triggering and adjust R61 for a negative-going pulse length of 20 μs ±1 μs.

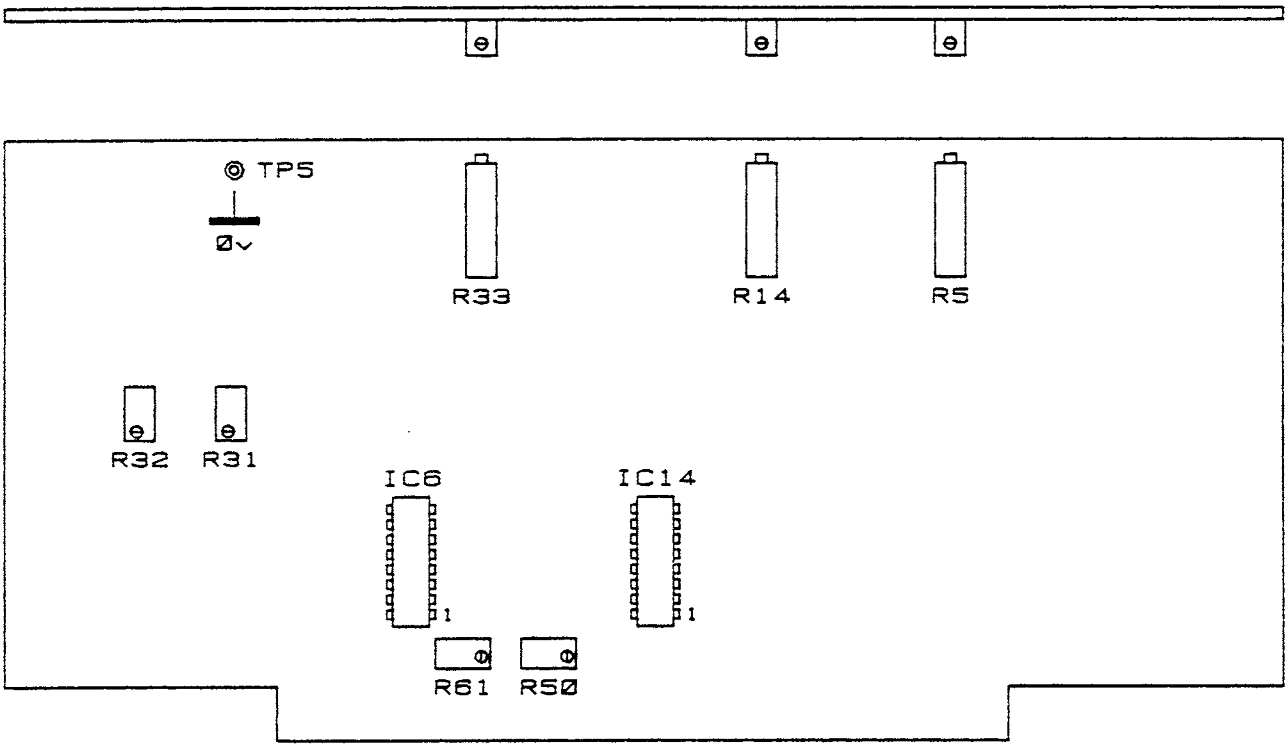


Fig. 8 Calibration component location chart (AC12)

Signal channel alignment (AC12/AF03/1)

Test equipment : items d, RF Power source
e, 50 MHz, 0 dBm Calibrator
f, Detector 6511 (Standard with calibration certificate)
g, Detector 6511 (General purpose)

69. Ensure that AT01/1 tray is screwed down and board AC12 is plugged into the card frame, also ensure that no extender cards are in use on any other board for the duration of this alignment. Switch on all test equipment on the 6500 and allow a 30 minutes warm-up.

Notes ...

(1) The standard 6511 should be maintained at the standard temperature of 22^0 C and should be handled as little as possible.

(2) Ensure that the AUTOZERO operations are carried out correctly with no r.f. applied.

(3) Familiarity with the CALAID facilities is essential before attempting the following alignment. Instructions on the use and operation of the facility can be found in the beginning of this chapter if required.

70. Set each of the following potentiometers to approx. mid-travel, location of these are shown in Fig. 8 and 9.

AF03/1	R105	(Channel ´A´ Sensitivity)
AF03/1	R205	(Channel ´B´ Sensitivity)
AF03/1	R305	(Channel ´R´ Sensitivity)
AF03/1	R119	(Channel ´A´ Range 2-3 level adj.)
AF03/1	R219	(Channel ´B´ Range 2-3 level adj.)
AF03/1	R319	(Channel ´R´ Range 2-3 level adj.)
AC12	R5	(Stage 2 Amp. gain)
AC12	R14	(Stage 3 Amp. gain)
AC12	R33	(Signal output level)

Connect a 6511 detector to the RF source and Channel ´A´ on the 6500, switch RF off and perform the AUTOZERO on the 6500. Check that no error is produced for Channel ´A´ - possible error messages are ´Fail´ (accompanied by Error 42) and ´No Probe´.

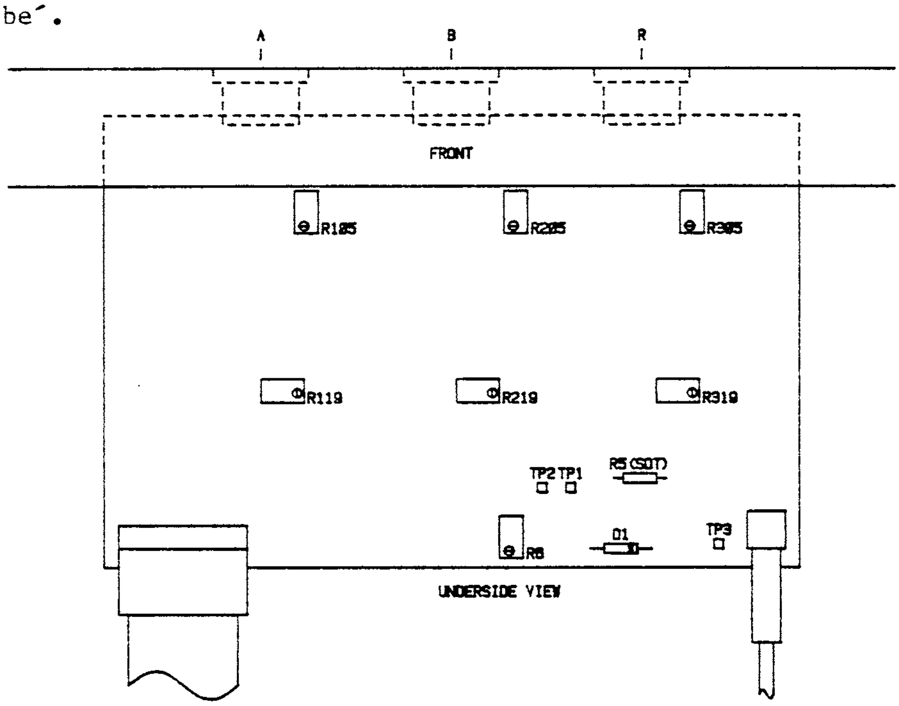


Fig. 9 Calibration component location chart (AF03)

71. Select CALAID, switch off the temperature correction and select Channel A. Switch the external RF source level on and adjust the level to give approximately -1 dBm on Range 1.

(1) Using the ´BAR CHART´ display and numeric information, adjust AC12,R14 to give identical readings on Ranges 1 and 2. At this point, the ´BAR CHART´ level will coincide with the reference line. Note that the response of the ´BAR CHART´ is deliberately slowed.

(2) Reselect Channel ´A´ on CALAID pressing numeral 7 to reset ´BAR CHART´. Wait 20 seconds for any deviation.

Note ...

The BAR CHART facility only operates when two adjacent ranges give readings. If only one range shows a valid reading re-adjust the RF level to obtain a reading on both ranges.

(3) Adjust the external RF source level to give approximately -16 dBm on Range 3, and adjust AF03/1,R119 to set up range change 2 to 3 using the BAR CHART.

(4) Adjust the external RF source level to give approximately -36 dBm on Range 5, and adjust AC12,R5 to set up range change 4 to 5 using the BAR CHART.

72. Connect the standard detector/calibrator box to Channel 'A' of the 6500. Then with calibrator r.f. level off perform the AUTOZERO function. Select the 6500 to DATUM 0.5 dBm, RANGE 0.1 dBm/div. then switch calibrator on, wait 30 seconds and adjust AC12,R33 to obtain a reading of 0 dBm. When this measurement is within ±0.03 dBm select AVERAGE to facilitate setting to within ±0.01 dBm. Take the reading from the brightline display at the top of the screen. Repeat the adjustments until reaching the optimum. Typically, no more than two repetitions will be required.

73. Channels 'B' and ('R') can now be set up in the following manner :-

(1) Connect the 6511 detector from the RF source (RF level off) to Channel 'B' ('R') on the 6500. AUTOZERO and check that no errors are displayed for Channel 'B' ('R'). Select SHIFT, CALAID and confirm that the temperature correction is OFF.

(2) Select Channel 'B' press numeral 8 (Channel 'R' press numeral 9) switch RF source level on and set for approximately -16 dBm on Range 3. Adjust AF03/1,R219, (AF03/1,R319) to set up Range change 2 to 3 using the BAR CHART.

(3) Connect the standard detector/calibrator box to Channel B (R). With the calibrator r.f. level off perform the AUTOZERO function.

(4) Select the 6500 to DATUM 0.5 dBm, RANGE 0.1 dBm/div. then switch calibrator on and wait 30 seconds. Adjust R205, Channel B (R305,Channel R) to obtain 0 dBm adopting the same technique used for Channel A adjustment i.e. Select AVERAGE when within ±0.03 dBm and carry out further adjustment to achieve an optimum reading within 0.01 dBm, repeating the adjustment to achieve the best possible reading.

Temperature sensor circuit calibration (AF03/1)

Test equipment : items 1, Resistance box connected via a 6511 probe connector to pin M. Temperature input connection and earth, pin J.
h, Digital voltmeter

74. Switch on all equipment and allow 30 minutes warm-up. Referring to Fig. 9 component layout for AF03/1, measure the Zener diode reference voltage D1 and re-select the value of resistor R5 if the voltage obtained and resistor value do not coincide with the value given in Table 3.

TABLE 3 TEMPERATURE SENSOR CALIBRATION (R5 SELECTION)

Zener reference voltage (Volts)	Value of SIC resistor (R5)
5.89 - 5.98	392 kΩ
5.98 - 6.12	402 kΩ
6.12 - 6.25	412 kΩ
6.25 - 6.39	422 kΩ
6.39 - 6.51	432 kΩ

75. Select Channel A. Plug resistance box and probe connector into Channel A front panel input socket and carry out the following procedure:-

(1) Adjust the resistance box for a voltage of -0.6000 volts between TP1 and ground (typical resistance value 43 kΩ).

(2) Adjust AF03/1,R6 for an output of +4.887 V ±0.003 V between IC6, pin 6 and ground. On completion remove resistance box and d.v.m.

FAULT LOCATION

76. The following section consists of a fault finding table and other checks to aid fault location. To assist with fault finding it is advisable to study the technical description contained in Chap. 4. The functions of the various boards are generally well defined and independent of each other. Boards/modules are interconnected by a variety of connectors. A useful method of confirming if board or module is faulty is to substitute with a known serviceable item from a spare working instrument. This can save considerable fault finding time.

77. When disconnecting conhex connections ensure that the metal clad connector cannot accidentally cause short circuits on the printed boards and create additional faults.

78. The checks given in this chapter are not exhaustive but are intended as a pointer to further investigation. It is emphasized that each fault should be studied having regard for other fault finding information, since incorrect operation of a circuit may be caused by malfunction of an associated circuit.

Power supply faults

79. Symptoms of power supply faults are often confusing therefore it is recommended that both primary and secondary fuses be checked before commencing any other tests. Investigate the cause of any fuse found to be blown. Note that +5 V and +12 V supplies do not have secondary fuses fitted. All voltages can be checked as described in the Adjustment and Calibration paragraphs.

Signal channel faults AF03/1

80. Faults involving the signal channel input board AF03/1 will normally be indicated on the display by a 'Fail' or a 'No probe' message when an attempt is made to carry out the AUTO ZERO procedure. Establish first by connecting

a detector probe to each input in turn, which of the three channels A, B or R is affected. Functional checks at the beginning of this chapter show the message normally expected when a detector probe is connected to each channel input in turn.

81. If one channel only is affected it is possible that the fault lies in that channel's Chopper or 1st stage amplifier. If board AF03/1 replacement is thought to be necessary it should be carried out with extreme care. Interconnections between each of the probes input sockets and the board are kept as short as possible to prevent noise pick-up. Fig. 10 indicates the interconnections between the probe input sockets, their pin connections and the board terminations. Also indicated are the wires that require sleeving.

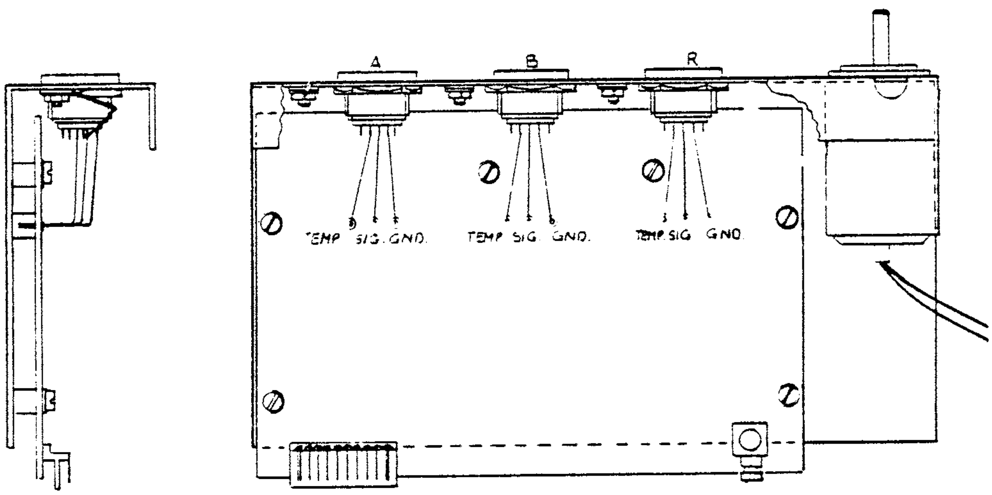


Fig. 10 Probe input sockets and AF03/1 board interconnections.

82. A list of possible faults associated with the Signal input board AF03/1 follow. These are by no means exhaustive but are rather meant as a guide to assist the user to determine the likely area of the defect.

(1) Fault symptom : 'No probe' on one channel only.

Possible fault : Short circuit between Probe input socket and AF03/1 board.

Check : That all connections to the input probe socket pins are correctly terminated and sleeved as shown in Fig. 10. Ensure that connections to pins B, M and L are not shorting to a chassis pin connection.

(2) Fault symptom : 'Error 42', 'Error 46' for one channel and/or 'Fail' indication on all three.

Possible fault : AF03/1 multiplexer IC5.

Check : Carry out the checks given for fault (1) or multiplexer IC5 operation.

(3) Fault symptom : 'No probe' on all three channels.

Possible fault : +15 V and +5 V supply missing on AF03/1.

Check : +15 V input at PL1 pin 10 and +5 V regulator output across C8.

(4) Fault symptom : 'Fail' on all channels and excessive noise on c.r.t. display.

Possible fault : AF03/1, IC2 defective, or AC09/2 Auto zero voltages missing.

Check : IC2 is serviceable, renew if in saturation. Check AC12 voltages on pins A21 & A30 vary when carrying out AUTO-ZERO routine. Using CALAID facility check that voltages are stable on any one range.

(5) Fault symptom : AUTO ZERO procedure on channel 'A' indicates 'No probe' on channel 'B'. Attempts to AUTO ZERO channel 'B' with a probe fitted also produce the 'No probe' message.

Possible fault : IC3 AND and/or IC4 NAND gates open circuit.

Check : That f.m.1 and f.m.2 signals are present at AF03/1, PL1, pins 1 and 2 and that f.m.2 positive-going transition leads f.m.1. by ≈1 μs. Check function of IC3, IC4.

(6) Fault symptom : 'Error 46' or 'No probe' message on all channels.

Possible fault : Open circuit component in AF03/1 temperature sensor.

Check : Temperature sensor components for open circuit particularly R5 and D1. Voltage across D1 should be in accordance with Chap. 5, Table 3, if necessary renew D1 and reselect R5. Check R6 is not intermittent.

(7) Fault symptom : 'Error 46' and c.r.t. display at ≈ +18 dBm.

Possible cause : -15 V supply missing.

Check : AR07,FS4 is intact, also check that -15 V is present across AF03/1,C7.

(8) Fault symptom : 'No probe' message on all channels.

Possible cause : AF03/1, TR1 open circuit.

Check : TR1 collector (can) is at +5 V and that TR1 inverter operates to switch IC102 1st stage attenuator, use CALAID on 'Cycle' operation.

(9) Fault symptom : 'No probe' message on either A, B or R channels.

Possible cause : AF03/1, IC5 failure, or incorrect logic applied.

Check : That -15 V is present on IC5 pins 4, 7 and 11 and that +5 V is present on pin 16. Check that logic inputs M0, M1 are correct for the selection of channels A, B and R, i.e.,

	M0	M1
A =	0	0
B =	1	0
R =	0	1

Check the function of IC5.

CRT/ATO faults

Test equipment items: a, Multimeter
b,c, Oscilloscope & probe
m, Electro-static voltmeter

⚠ WARNING LIVE PARTS ⚠

83. Before attempting to trace faults in this area it is essential that the relevant Notes and Cautions have been read at the front of this manual. Also read the WARNINGS in this chapter relating to access and correct servicing procedures when working in this area.

84. Before carrying out any electrical tests inspect all soldered connections for dry joints etc. The following list of fault symptoms and remedies give information and typical waveforms that can be monitored on board AT01/1,AT02, and the c.r.t. These can be seen in Fig. 11. Note that all waveforms and voltages are measured with respect to TP2.

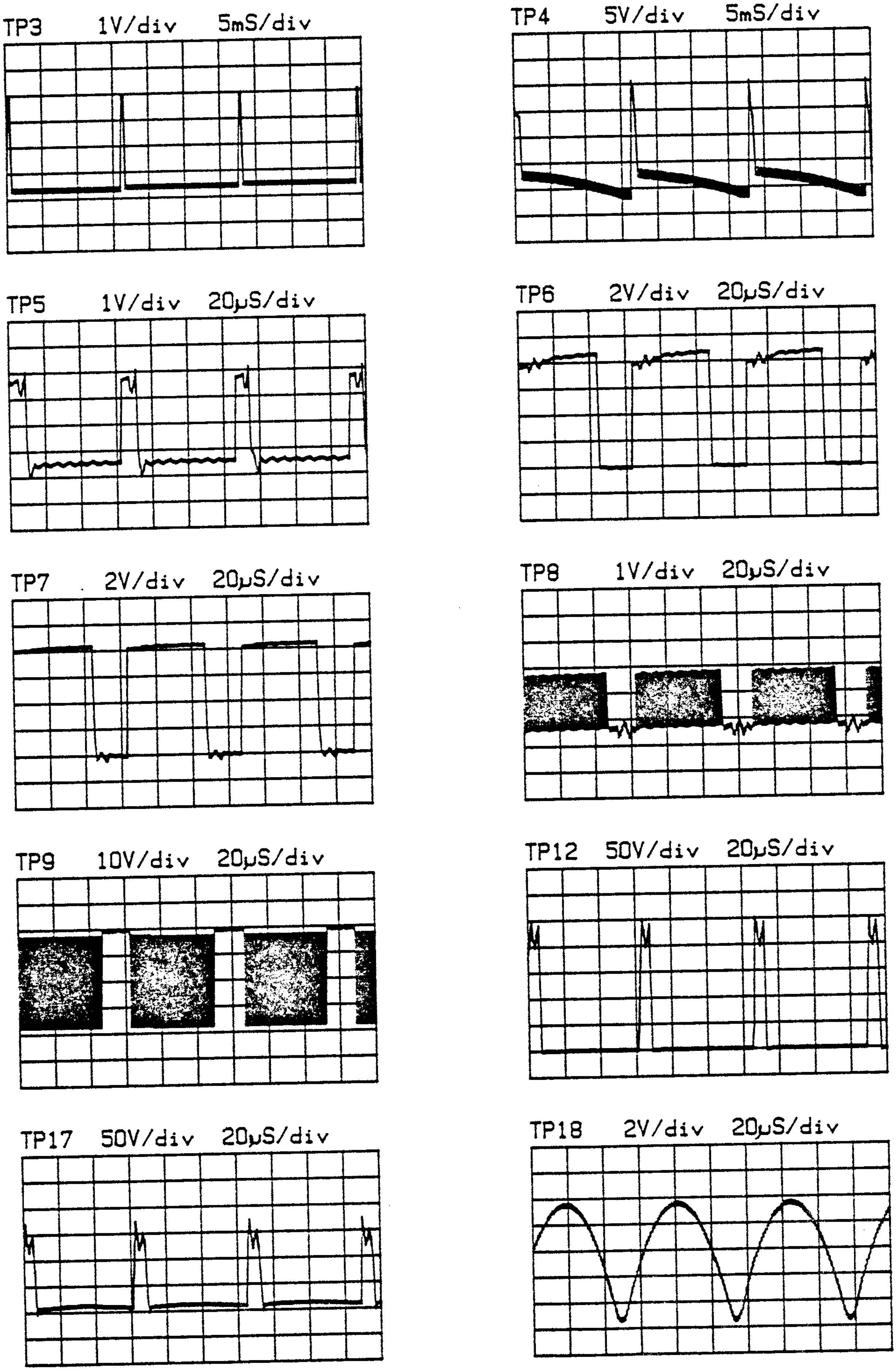


Fig. 11 Typical waveforms AT01/1

(1) Fault symptom : No video present, but synchronized raster.

Possible cause : Poor connection to c.r.t. cathode.

Check : Waveform at TP9 appears at c.r.t. pin 2.

(2) Fault symptom : No video, unsynchronized raster.

Possible cause :
(i) Suspect video input connections
(ii) No 100 V HT
(iii) No output from video amplifier

Check :
(i) Waveform at TP8 then at TP9.
(ii) Voltage at TP13
(iii) TR1,TR2,TR3 for serviceability

(3) Fault symptom : Video not clamping to black level.

Possible cause :
(i) Input level to video amplifier could be too high
(ii) Line sync. pulse width too wide
(iii) TR2 bias level incorrectly set

Check :
(i) Waveform at TP8
(ii) Waveform at TP5
(iii) DC level (+70 V) at TP9

(4) Fault symptom : No line hold.

Possible cause :
(i) No line sync input
(ii) IC2 not operating
(iii) IC3 not operating

Check :
(i) Waveform at TP5
(ii) Waveform at TP6
(iii) Waveform at TP7

(5) Fault symptom : No frame hold.

Possible cause :
(i) No frame sync input
(ii) Frame lock control (R48)
(iii) IC1 faulty

Check :
(i) Waveform at TP3
(ii) R48 for open or intermittent circuit
(iii) IC1 for serviceability

(6) Fault symptom : No frame scan.

Possible cause :
(i) Frame amplitude control (R3)
(ii) Coupling capacitor C10
(iii) Scanning coil L3
(iv) IC1 faulty

Check :
(i) R3 for open or intermittent circuit
(ii) C10 for leakage etc.
(iii) Continuity of frame windings - resistance should be approx. 3 Ω.
(iv) IC1 for serviceability

(7) Fault symptom : Excessive width.

Possible cause :
(i) High HT
(ii) Frame amplitude control (R3)
(iii) IC1 faulty

Check :
(i) +12 V rail at TP1
(ii) R3 for open or intermittent circuit
(iii) IC1 for serviceability.

(8) Fault symptom : Low width.

Possible cause :
(i) Low HT
(ii) Frame amplitude control (R3)
(iii) IC1 faulty

Check :
(i) +12 V rail at TP1
(ii) R3 for open or intermittent circuit
(iii) IC1 for serviceability

(9) Fault symptom : Poor frame linearity.

Possible cause :
(i) Frame linearity control (R6)
(ii) Coupling capacitor C10
(iii) Deflection coils L3
(iv) IC1 faulty

Check :
(i) R6 for open or intermittent circuit
(ii) C10 for leakage etc.
(iii) Replace L3
(iv) IC1 for serviceability.

(10) Fault symptom : Localized non-linearity (several lines widely spaced).

Possible cause : IC1 faulty

Check : IC1 for serviceability.

(11) Fault symptom : Excessive height.

Possible cause :
(i) High HT
(ii) Frame amplitude control (L1)
(iii) Frame linearity control (L2)
(iv) Low EHT.

Check :
(i) +12 V rail at TP1
(ii) Adjustment or replacement of L1
(iii) Adjustment of L2 for best linearity
(iv) Line output stage as detailed in fault symptom (17).

(12) Fault symptom : Low height.

Possible cause :
(i) Low HT
(ii) Frame amplitude control (L1)
(iii) Frame linearity control (L2)
(iv) Boost volts low.

Check :
(i) +12 V rail at TP1
(ii) Adjustment or replacement of L1
(iii) Adjustment of L2 for best linearity
(iv) 27 V at T1 pin 10, if incorrect check reservoir capacitor C25 and diode D5.

(13) Fault symptom : Poor line linearity.

Possible cause :
(i) Frame linearity control (L2)
(ii) S Correction capacitor C30)
(iii) Slow switch off of TR6
(iv) Yoke of L3.

Check :
(i) Adjustment of L2
(ii) C30 for leakage etc.
(iii) Waveform at TP12, if incorrect check TR6, and L3 for serviceability.

(14) Fault symptom : Poor corner focus performance.

Possible cause :
(i) Focus potentiometer (R44)
(ii) Scan coil (L3)
(iii) Incorrect c.r.t. volts
(iv) CRT.

Check :
(i) Adjustment of R44
(ii) Serviceability of scan coil L3
(iii) Line output stage as detailed in fault symptom (17)
(iv) CRT for serviceability if all voltages are correct.

(15) Fault symptom : Bent horizontals.

Possible cause : (i) Power supply current limit set too low
(ii) HT de-coupling
(iii) Raster centring
(iv) Picture shape.

Check : (i) Limit to 1.5 A
(ii) C1 for leakage etc.
(iii) Adjustment of shift rings on L3
(iv) Adjustment of shape magnets on L3.

(16) Fault symptom : Uncontrollable and excessive brightness.

Possible cause : (i) Video amplifier - TR1,TR2,TR3
(ii) CRT (cathode or grid short)

Check : (i) TR1,TR2,TR3 for serviceability
(ii) CRT for serviceability.

(17) Fault symptom : No visible raster.

Possible cause : CRT voltages.

Check : This fault requires a different check procedure because if the line output stage is not functioning, other d.c. voltages normally supplied to other stages of the circuit will be absent.

Procedure

(1) Check +12 V rail at TP1. If incorrect disconnect D5 and if +12 V returns, suspect line output stage components TR6,D10,D7,C25,C26,D5. If +12 V does not return suspect TR2,TR3 or IC1.

(2) If +12 V rail is correct check waveform at TP12:-
and/or 27 V boost at T1 pin 10
and/or +100 V at TP13
and/or +150 V at TP11.

(3) If all voltages to step (2) are correct and TP12 waveform is also correct check the c.r.t. operating voltages at the tube base as follows:-

h	Is heater alight? (examine in subdued lighting)
al	+150 V at c.r.t. pin 6, if not suspect c.r.t. connection
k	65-75 V d.c. at c.r.t. pin 2, if not suspect c.r.t. connection.
g	-50 to +30 V at c.r.t. pin 1 as R46 is varied, if not suspect c.r.t. connection.

a4 11.5 to 12.5 kV on c.r.t. anode, if not suspect overwind on T1.

Note ...

Do not check by drawing off a spark from the e.h.t. connector.

(4) If c.r.t. voltages are incorrect suspect TR6,IC2,IC3,D5,C28,TR2 and TR3, then all other line output components.

CRT replacement

85. Remove both top and bottom front trim strips, hinge AT0 lid and fix this into the servicing position. Remove the c.r.t. socket and base sparkguard AT02 (there is sufficient length on the earth lead from AT02 to braid to allow removal of the c.r.t. with the braid attached) take care not to fracture the neck of the c.r.t.

86. Loosen the scan coil yoke assy. neck clamp securing the assy. to the c.r.t. and draw assy. off towards the rear.

87. Unlock the elasticated rubber fixing strap from the two upper lugs and also detach the earthing assy. from around the fixing bands. Carefully lift the c.r.t. from the gasket and dispose of it as detailed in the beginning of this chapter.

88. Take the replacement c.r.t. from its packaging, leave the pin protector and the plastic sheet on the tube face. Place the c.r.t. on its face in front of the unit with the anode on the left hand side on to a protected surface (e.g. rubber mat). Clean the anode area with a residue free cleaner (industrial methylated spirit) and also clean the anode cap on AT02.

89. Ensure that the elasticated rubber fixing strap is attached to the lower fixing point and that the rivet coupling is centrally positioned. Carefully remove the plastic sheet from the tube face and place the c.r.t. into the gasket and re-attach the fixing strap to the two upper mounting lugs to hold the c.r.t. firmly in position. Re-attach the earthing assy. ensuring that the earthing makes good contact with the c.r.t.

90. Refit scan coil assy. c.r.t. anode cap, board AT02.Finally remove the pin Orprotector from the c.r.t and fit the c.r.t. plug. Carry out the c.r.t align- ment in the manner described in Adjustment and Calibration paras.

Processor faults (AC18) - Self test fault displays

91. If a ROM or RAM fault is suspected, or is indicated on the display as a self test fault, note the qualifying address and identify the IC concerned by reference to Chap. 7 Servicing diagram's memory map. Switch the instrument off and withdraw the board. Visually inspect this paying particular

attention to the IC whose memory address has been indicated on the display. Press suspected ICs at both ends to firmly seat them into their sockets. Remove the board and clean the edge connector with a residue free cleaner (industrial methylated spirit) then firmly replace the board ensuring the correct orientation.

92. Switch on - if the fault persists, try slightly removing the IC from the socket and pushing back in, taking care not to damage the pins - this is only likely if the IC is completely removed and re-inserted. Similarly other boards that could exhibit a memory fault are the following,

	AC02	Address 50XX onwards		D0XX	onwards on Link
Link option One (AC18)	AC03	Address 54XX onwards	or	D4XX	options Two or
	AC04/1	Address 5CXX onwards		DCXX	Three (AC18)

Fault conditions will be clearly displayed on the c.r.t. at power-on when the Self test operation is carried out. The operation is described in the Operating Manual Vol. 1 Chap. 3-1 "Preparation for use". Two typical faults exhibited by the 6500 are as follows :-

(1) PORT FAULT 0, 8080 (keyboard data port)
Bit 0 stuck on 8080H indicates that the microprocessor cannot detect the keyboard scanning.

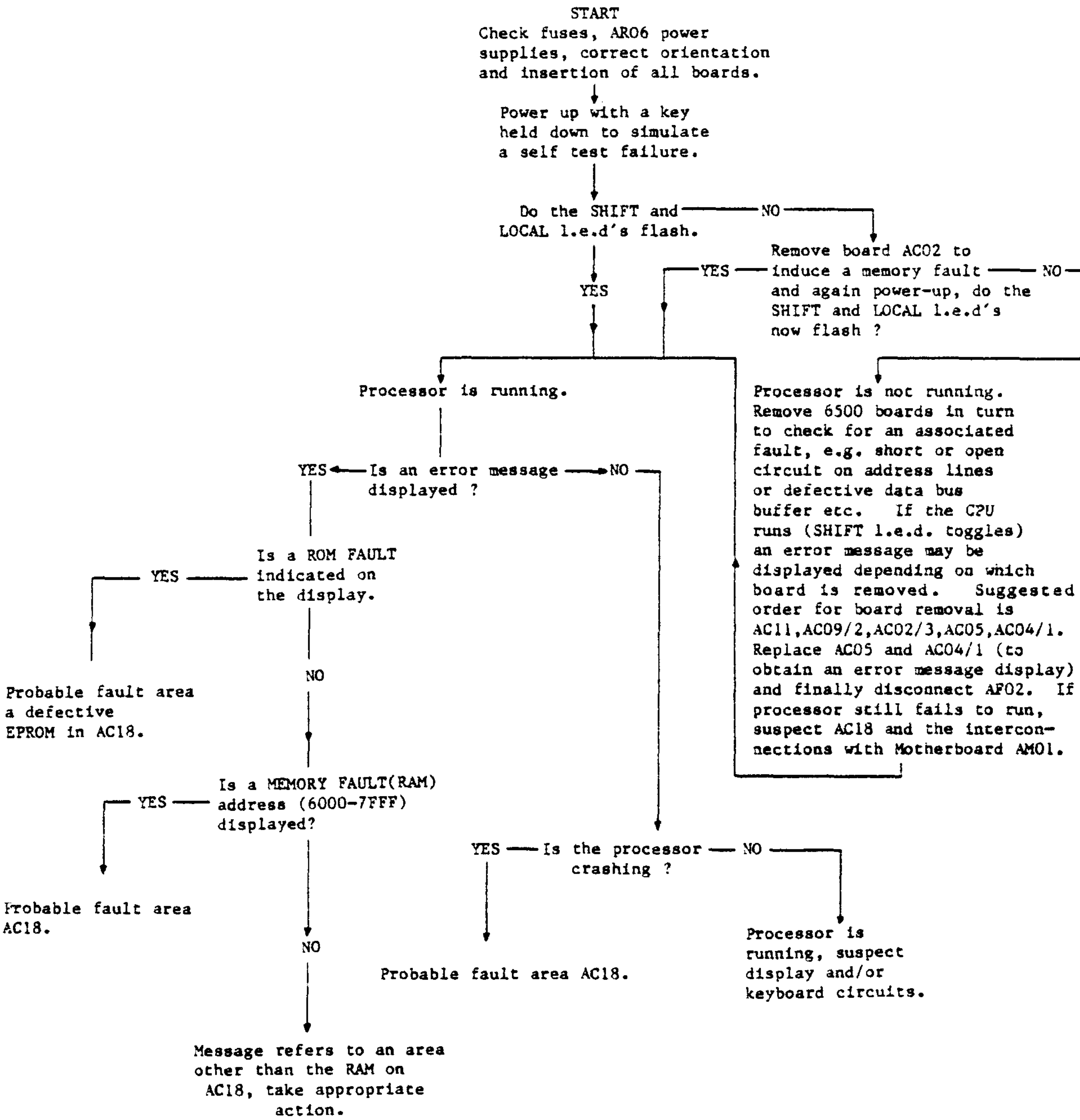
Possibilities :-
(1) Key jammed
(2) Connection to AM01
(3) Power supply unit AR06
(4) Encoder AF02 (IC1)
(5) Keyboard data port AF02, IC8.

(2) PORT FAULT 0, 8803
Bit 0 stuck on 8803H indicates that no ADC end-of-conversion pulse is present.

Possibilities :-
(1) No power applied to board AC11
(2) ADC START CONVERSION pulse from AC12 missing or incorrect.
(3) CONVERT PULSE to AC11, IC3 missing
(4) A-D converter IC3 on AC11 suspect.

If a Memory (RAM) fault occurs during use, a message is written on the display to indicate this. The indication can be in the form of a Memory or Hardware error message or alternatively as a Memory fault with an identifying address. See also Table 4 for typical processor fault finding procedure.

TABLE 4 PROCESSOR FAULT FINDING PROCEDURE



<u>Display faults</u>

93. The faults described in this paragraph are those which are seen on the display but which are caused generally by faults not directly associated with actual display board AT01/1 or AT02.

(1) Fault symptom : Transient video glitches present on Display trace(s).

Possible cause : Microprocessor access de-glitch circuit AC02/3, IC5 maladjusted.

Check : The adjustment of the de-glitch circuit AC02/3 R1 and R2. If the fault is still present after adjustment suspect IC5, substitute with a known serviceable item.

(2) Fault symptom : Incorrect data present on MEMory displays (Memories should contain all 0.00 dBm points unless a STORE operation has been performed).

Possible cause : Intermittent connections on AC18 edge connectors or an intermittent RAM, IC.

Check : AC18, RAMs, seating of each IC and p.c.b. connections, also clean and check edge connector pins for a good connection in the card frame. Run Diagnostic ROM - replace any faulty ICs indicated by the program. Replace AC18 board if fault persists. When fault appears to be corrected, power up and down the instrument a number of times to ensure that the fault does not re-occur.

(3) Fault symptom : Striations (bands of varying intensity) on the screen.

Possible cause : AT01/1,AT02 wiring loom incorrectly positioned.

Check : That the position of the wiring loom is such that mutual coupling between loom and AT01/1 module M2 is minimized.

(4) Fault symptom : Jittering alphanumerics on left hand side of display.

Possible cause : AC01 incorrect interlace adjustment.

Check : Alignment of the interlace control R8.

(5) Fault symptom	:	Excessive noise floor level on display i.e. > -50 dB.
Possible cause	:	AF03/1, buffer IC2.
Check	:	By substituting IC2 with a known serviceable item.
(6) Fault symptom	:	Line display trace which should be located off the top of the screen, is partially visible e.g. power on displays 50-60 dB. Set DATUM to -99 dBm, display to LINE.
Possible cause	:	Incorrect adjustment of line display clock circuit, AC01 board.
Check	:	The alignment of the line display clock oscillator AC01, R11.

Chapter 5-1

DETECTOR MAINTENANCE (6511/6512)

CONTENTS

INTRODUCTION

1. This chapter contains information to assist in the repair and test procedures of Wide band detectors, if required. The procedures described in this chapter are of a simplified nature and of restricted range compared with those that relate to the more comprehensive factory test facilities which are necessary to demonstrate complete compliance with the specification.

2. The detector requires careful handling and comprehensive v.s.w.r. and power accuracy checks and because of this it is recommended that repair and re-calibration be carried out only by authorized Marconi Instruments agents or by Marconi Instruments, Microwave Products Division, Stevenage.

Detector servicing ⚠ (Static sensitive device - see Notes & Cautions)

3. If specialized equipment is available to the user or it is accepted that repairs may be carried out without the detector being calibrated to its full specification the following instructions given in this chapter will enable the replacement of three sub-assemblies that may be changed without the use of special tools. A list of available spare parts is shown in Fig. 7 and access to some of these require special tooling. It is therefore recommended that dismantling beyond the sub-assembly stage is not attempted in the course of normal servicing. The three sub-assemblies available are as follows :-

(1) 6511, RF connector assy. N type, Part No. 2716-007
or 6512, RF connector assy. APC-7 type, Part No. 2718-007

(2) Cable assy. (includes 12 pin male connector) Part No. 2716-004, details are also supplied showing wiring details of both p.c.b. and plug interconnections, see Fig. 4.

⚠ (3) Detector module assy. kit Part No. 2716-006
(The kit includes two pre-selected (SIC) resistors, R2 and R6).

4. Two sets of instructions are given in the following paragraphs to enable calibration to be carried out. The first gives a restricted routine using only two items of the test equipment listed in Table 1 : a, 50 MHz, 0 dBm calibrator and h, a 6500 in this procedure. The power accuracy setting is however limited by the uncertainties of the 6500. A second more detailed test procedure provides for greater power accuracy. A limited v.s.w.r. check (8.0 - 12.4 GHz), and a frequency response confidence check may also be carried out in addition if all the items listed in Table 1 are available.

Module replacement ⚠

5. Fig 1 shows the circuit diagram of the detector module, p.c.b. and wiring details. Fig. 2 shows an exploded view of the detector to assist in the dismantling which can be carried out as follows :-

(1) Remove the two rear plate fixing screws and slide the rear plate and casing down the cable towards the plug.

(2) Progressively remove the three socket headed fixing screws securing the module retainer in position, hold the module retainer and with an axial action (i.e. a straight pull) gently detach the r.f. connector assy.

6. The module can now be removed from the retainer, this should also be withdrawn with an axial action and under no circumstances must a twisting action be exerted during withdrawal. It may be necessary to grip the end of the module with pliers or similar, using a suitable amount of padding to ensure that the plated surface is not damaged. The module assembly contains exposed chip devices that are static sensitive, they are also connected with

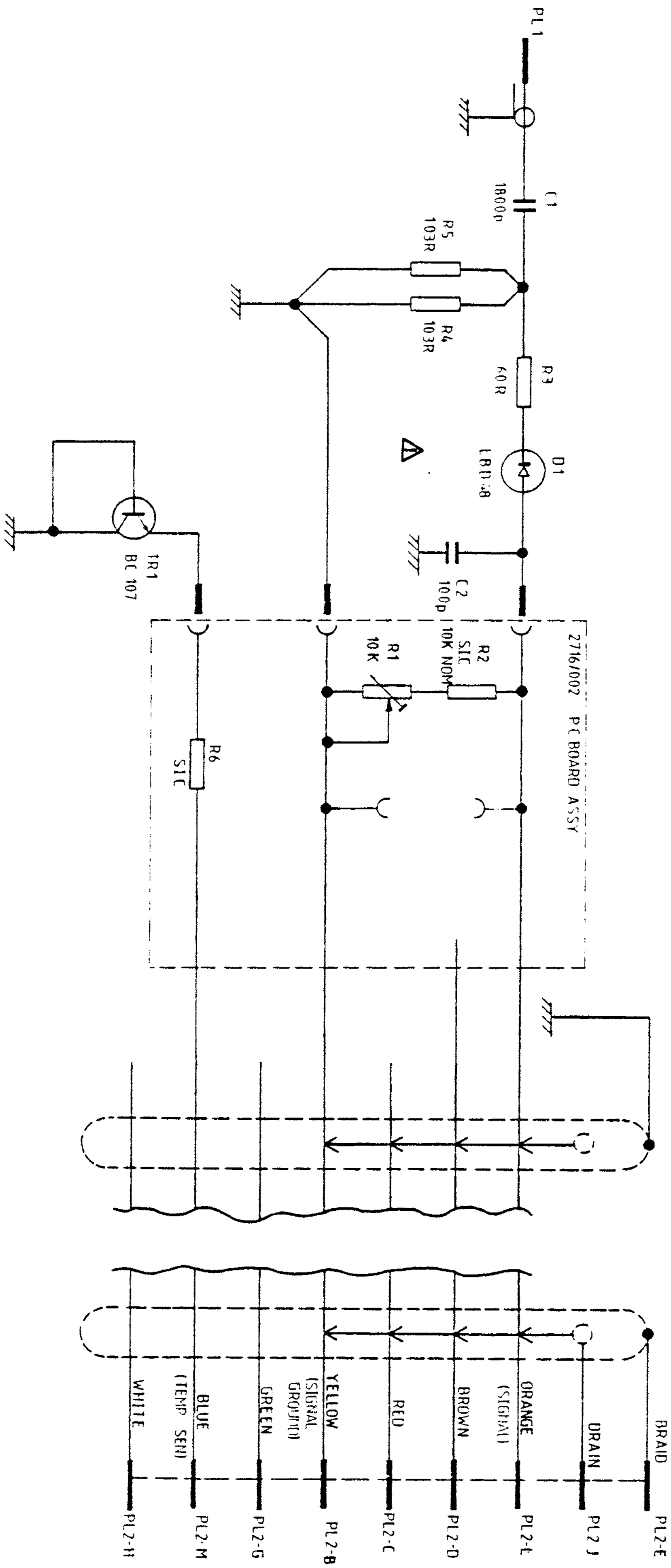


Fig. 1 6511(6512) Detector circuit diagram

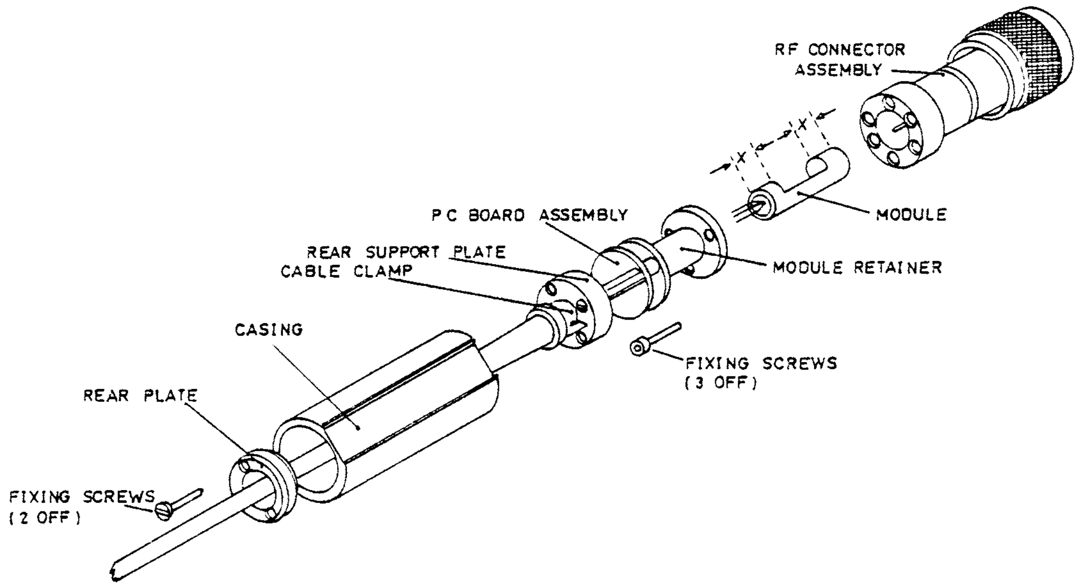


Fig. 2 6511 Detector, exploded view

a fine bond wire and therefore should not be handled directly. Instead hold the module casing across the X dimensions and withdraw the module by purchasing only from the edges.

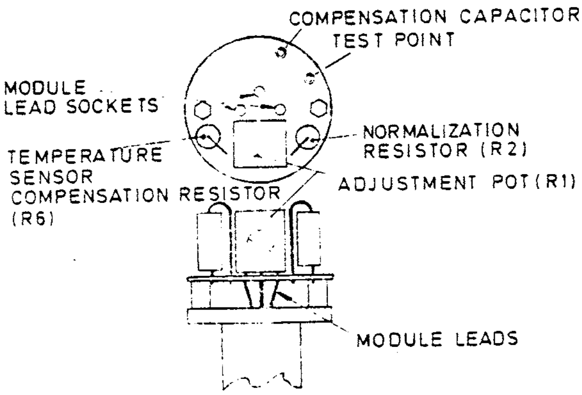
Note ...

> During withdrawal particular attention should be given to the positioning of the three contact wires so that the replacement item can be inserted into an identical position. Without care it is possible to connect the wires incorrectly.

Module replacement kit

7. Note the value of resistors included with the detector module replacement kit, if either of these differ in value to resistors R6 and or R2 mounted on the p.c.b. and shown in Fig. 3 they must be replaced by those supplied in the kit. Using a fine tip soldering iron remove either or both resistors, (R2) normalization, and (R6) temperature sensor compensation, with the minimum possible heat applied. Solder using flux cored 60/40% tin, lead solder. Remove any locking compound from the adjustment potentiometer (R1) to allow for subsequent re-calibration.

8. Gently push the replacement module into the retainer locating the three connecting wires with the correct module lead sockets of the p.c.b. as shown in Fig. 3. Being careful to retain the axial alignment insert the module into the r.f. connector assy. Replace the three module retainer screws and progressively tighten these, use Locktite 222 or similar to lock the threads of each screw.



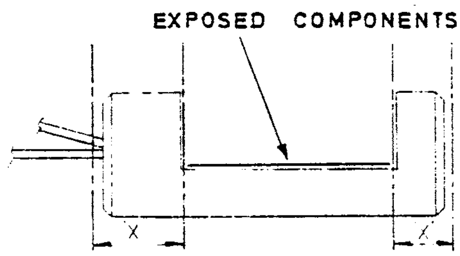


Fig. 3 PCB assy. diagram

TABLE 1 TEST EQUIPMENT

Item	Description	Minimum use specification	Recommended model
a	50 MHz 0 dBm Calibrator	With current calibration certificate 1 mW ±0.7%	Available on Power meters 6950 or 6960
b	Digital volt-meter	DC volts : 0.1 V - 100 V Accuracy : 0.001%	
c	Signal source with Sweeper mode	Freq. range : 8.0 - 12.4 GHz Sweep capability : 0- +10V full sweep	6158A
d	Temperature sensor	$\pm 1^0$C	Comark thermometer (6600)
e	High directivity coupler or bridge		2200/327
f	Power splitter		HP 11667A
g	Detector 6511 (6512)(General purpose)	Specification as laid down in H 6500 Vol. 1, Chap. 1. (2 off)	
h	Automatic amplitude analyser	H 6500 Vol. 1, Chap. 1	6500
		Special tools and alignment aids	
i	Connector socket	12-way female Type 680-09-0330-00-12	MI (Microwave products)

Limited calibration (using only 0 dBm Calibrator and 6500)

Test equipment : items a,h

9. Connect the 6511(6512) Detector to the 50 MHz, 0 dBm calibrator and to Channel A of the 6500. With the r.f. source switched off carry out the AUTO ZERO function then if satisfactory switch on the r.f. source and with the 6500 temperature correction on set the 6511 adjustment potentiometer (R1) to give a reading of 0 dBm ±0.05 dB on the 6500. The adjustment should be carried out after allowing the ambient temperature to stabilize at 22°C or as near as possible for at least two hours. On completion lock the potentiometer with Silastic 732 silicone adhesive/sealant or similar.

10. Re-assemble the casing and backplate, sliding this over the detector and butting up to the r.f. connector assy. Locate the cable clamp in the slot on the rear support plate and slide the rear plate into position on the casing. Align rear support plate and rear plate screw holes, fit and progressively tighten the two chrome fixing screws locking these with Loctite 222 or similar.

Alternative calibration providing greater accuracy

Test equipment : items a,b,d,h,i

11. Interconnections between the d.c. output of the detector and the d.v.m. can most easily be made via a female 12 contact socket (item i). Wires should be soldered to the following pins of the socket and the free ends connected to the d.v.m. as follows :-

Socket pin no.	DVM terminal
Pin L (signal)	Positive terminal
Pin B (signal ground)	Negative terminal
Pin E (chassis, earth)	Remote guard terminal

12. Two further compensating components are required to carry out the calibration :

(i) 1 μF tantalum bead capacitor Part No. 26486-209F.
This should be inserted into the compensation capacitor test point, the position of which is shown in Fig. 3.

(ii) 39 kΩ 2% 1/4W resistor Part No. 24773-311A.
This should be connected across the d.v.m. +ve and −ve terminals to simulate the 6500 chopper load.

13. Also connect the r.f. input of the detector to the 50 MHz, 0 dBm calibrator in an area where temperature changes can be avoided. Monitor the temperature around the detector unit and leave for two hours for the unit to stabilize. When a stable temperature reading, within the range shown in Table 2 (ideally 22°C) has been maintained, set adjustment potentiometer (R1) to give a d.v.m. reading corresponding to the temperature reading shown in Table 2. On completion remove the compensating capacitor and lock the potentiometer with a suitable adhesive such as Silastic 732 silicone adhesive/sealant. Reassemble the casing and backplate as previously described in para. 10.

TABLE 2 TEMPERATURE/mV CHART

TEMPERATURE ^{0}C	CALIBRATION mV
17	202.5
18	202.7
19	202.8
20	202.9
21	203.0
22	203.0
23	203.0
24	203.0
25	202.9
26	202.8
27	202.8

CABLE ASSY. AND R.F. CONNECTOR REPLACEMENT

14. To renew either an N type (6511) or an APC-7 (6512) r.f. connector assy. simply remove the casing and the r.f. connector assy. as described in previous paragraphs . It is not advisable to further dismantle the r.f. connector, this requires special tools and the replacement of individual components is difficult.

15. The cable assy. includes the 12 pin male connector and therefore only requires connections to be made at the p.c.b. However Fig. 4 gives details of the interconnections to both p.c.b. and the 12 pin male connector should the user require to change only the plug and not the complete cable assy.

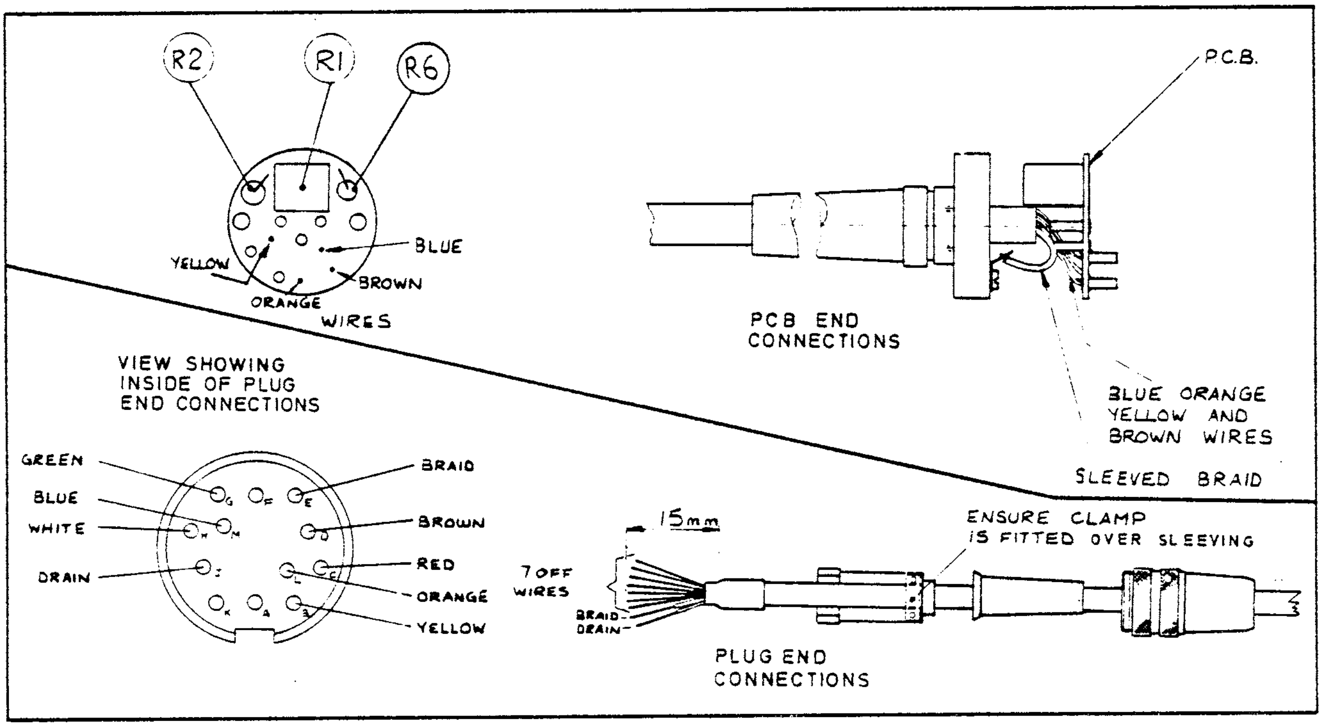


Fig. 4 Cable assy. wiring details.

DETECTOR FUNCTIONAL CHECKS

Temperature sensor check

Test equipment : items d,h

16. On completion of detector calibration the item should be fully cased for all subsequent confidence checks. When handling the detector take care to touch only the cable and not the body of the item. Connect the detector to Channel A of the 6500 and carry out the AUTO ZERO function, if this is satisfactory further select SHIFT and CALAID keys to display the temperature indication. With reference to Table 3 check that the 6500 temperature sensor figure displayed is within $\pm 2^{0}$C of the figure monitored at the detector by the thermometer.

TABLE 3 TEMPERATURE SENSOR FIGURES

6500 dBt Temp. reading	Temperature ^{0}C
2.2	27.9
2.3	26.9
2.4	26.0
2.5	25.1
2.6	24.2
2.7	23.3
2.8	22.5
2.9	21.7
3.0	20.9
3.1	20.1
3.2	19.3
3.3	18.6
3.4	17.8
3.5	17.1

VSWR confidence check

Test equipment : items c,e,f,g,h

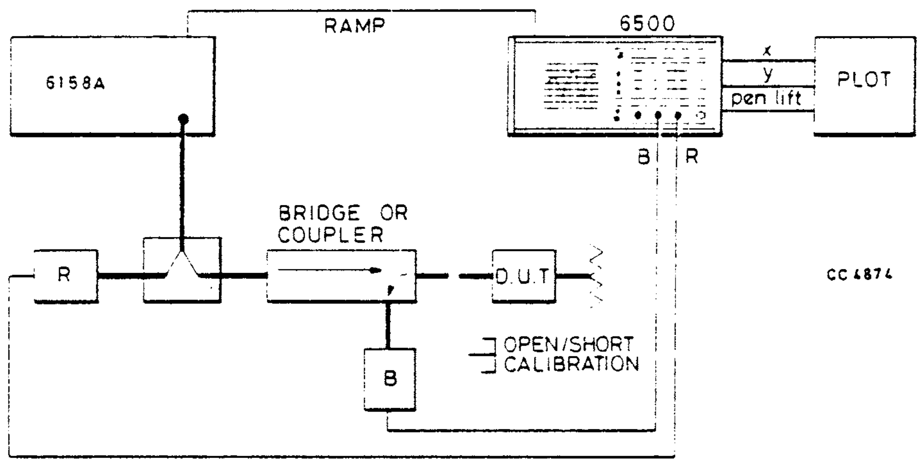


Fig. 5 VSWR measurement, interconnecting diagram

17. Connect the test equipment as shown in Fig. 5 and switch 6158A r.f. level off, and mode to SWEEP. Carry out the AUTO ZERO function on the 6500, if this is satisfactory complete the following :-

(1) Set the 6158A to sweep 8.0 - 12.4 GHz by entries on the 6500 F1 and F2.

(2) Switch 6158A r.f. source on and adjust the level to give an output at the bridge test port of 0 dBm.

(3) With OPEN CIRCUIT termination to the bridge select B, -R, STORE-B, on the 6500. Then fit SHORT CIRCUIT to the bridge and select SHIFT, STORE AV, B, on the 6500 (see Vol. 1, Chap. 3-2, Applications for further details).

(4) Connect the detector to be measured to the bridge test port and select SUB MEM,B and AUTO keys, the display now shows the return loss of the detector, pressing UNITS key will give a v.s.w.r. reading. Check that this does not exceed 1:1.35 across the range 8.0 - 12.4 MHz.

Frequency response check

Test equipment : items c,f,g,h

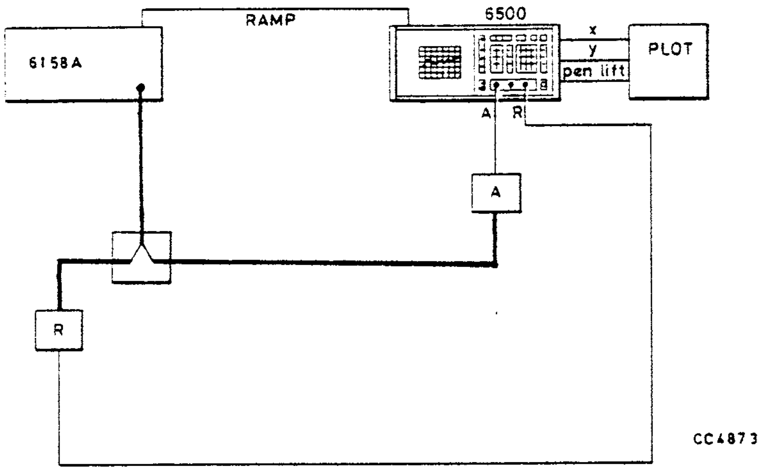


Fig. 6 Frequency response, interconnecting diagram

18. Connect the test equipment as shown in Fig. 6, switch 6158A r.f. source off and mode to SWEEP. Repeat the 6500 AUTO ZERO function, on completion switch 6158A r.f. source on and set the level for an output at the power splitter measurement port of -10 dBm, then carry out the following steps :-

(1) Store trace in memory using a known serviceable detector in Channel A.

(2) Replace Channel A detector by the repaired item and subtract new display from Channel A memory.

(3) Check that any variations in the resultant display do not exceed 1 dB.

SPARES

19. The number of spare items available for maintenance purposes are of necessity limited due to the minute size of some individual items and the difficulties involved in renewal of these. The following list of available spares therefore is not inclusive.

Fig. 7 Item	Description	Mfr./Part number
	Unit 6511/6512 Detector (wide band)	
	Complete item 6511	2716
	Complete item 6512	2718
1	RF connector assy. N type (6511)	2716-007 *
1	RF connector assy. APC-7 type (6512)	2718-007 *
1	Body moulding assy.	2716-001
2	Spring	2717-019
3	Plunger	2717-017
4	Centre contact assy.	2716-003
5	N type plug with 7 mm airline (6511)	131-10003
5	APC-7 type plug with 7 mm airline 6512)	131-1050
6	Sleeve	2716-012
7	Screw Zinc plate, Skt. Hd. M2 x 5 mm	GKN
8	Retainer (Module)	2716-014
9	Detector module assy. kit (includes R2,R6)	2716-006 *
10	Casing	2716-021
11	Screw, Zinc plate, Pan Hd. M2 x 10 mm	21837-241E
12	Spacer (short)	2716-018
13	Spacer (long)	2716-017
14	Printed circuit board assy. (includes Cable assy.)	2716-002
	PCB detail	2716-030
	Single contact connector socket	28488-004E
	Resistor variable (R1) 10K 0.5W ±20%	BOURNS 3329W-1-103 or SPECTRO RELIANCE
15	Plate (retaining cable)	2716-019
16	Screw, Zinc plate, Pan Hd. M2 x 8 mm	21837-239V
17	Screw, Chrome plate, Pan Hd. M2 x 12 mm	21838-243T
18	Cable assy. (Part of Printed circuit board assy.)	2716-004 *
	7 core double braid cable (2 M)	2716-500
	Rear plate	2716-020
	12 pin male connector	680-09-0329-00-12
	'0' clip W.107 1/4"	GRIFLEX

* Recommended
replaceable spare assys.

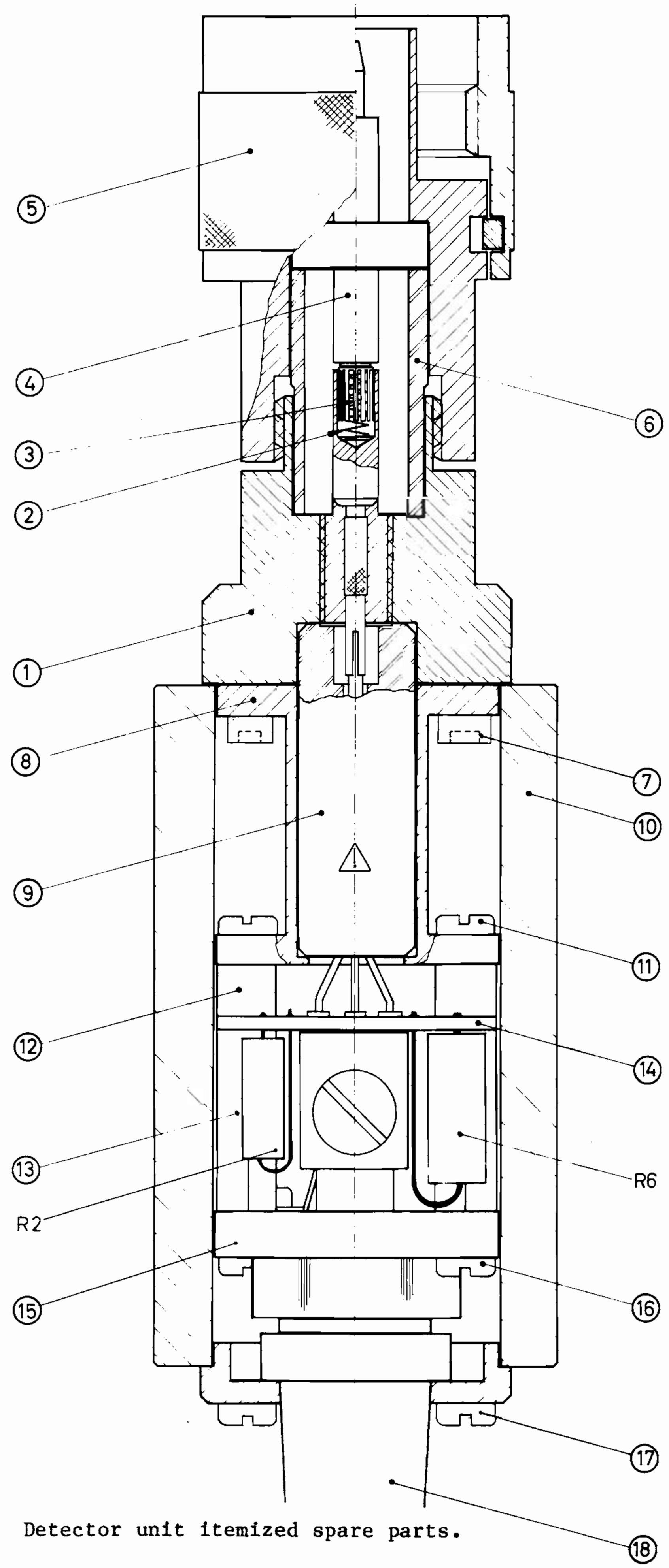


Fig. 7 Detector unit itemized spare parts.

Chapter 5-2

DETECTOR MAINTENANCE (6514)

CONTENTS

INTRODUCTION

1. The RF Detector 6514 is designed for use with 6500 Automatic Amplitude Analyser. The performance of waveguide assemblies may be characterized for transmission loss or gain, power, return loss or VSWR from 26.5 to 40 GHz over a 61 dB range.

OPERATION

2. Each RF Detector comes complete with waveguide attachment for user convenience and to avoid the possibility of damage to detector input face and screw threads through repeated attaching and detaching.

3. The 6514 detected signal is processed by the 6500 to produce a power reading. Powers outside of the square law of the diode are corrected by means of a look-up table in the 6500. The detector type function, DET, is used to select the correction for 6514. (Earlier instruments not having this key fitted can be retrospectively modified if this is required). Details for selecting the 6514 detector, zeroing, and setting of frequency limits are all described in the Vol. 1 Operating Manual.

MAINTENANCE

4. User servicing is not recommended for this detector and no itemized spares are available. If servicing is required the device should be returned to Marconi Instruments Microwave Products, Stevenage with details of any faults encountered.

PERFORMANCE TESTS

5. The following procedure will allow the user to verify the performance of the detector. This procedure is of a simplified nature however and of restricted range compared with tests that relate to the more comprehensive factory test facilities which are necessary to demonstrate complete compliance with the specification.

TABLE 1 TEST EQUIPMENT

Item	Description	Minimum use specification	Recommended model
a	Automatic amplitude analyser	See H6500 Vol. 1 Chap. 1	6500
b	Detector 6514	See H6500 Vol. 1 Chap. 1	6514
c	High directivity couplers	Directivity: >35 dB 26.5-40 GHz	HP R752C 2 off
d	Variable attenuator	26.5-40 GHz	6052/1
e	Signal source	Frequency: 26.5 - 40 GHz Output: 0 dBm	6600A/1
f	Power head/meter	Calibrated at 0 dBm at 33 GHz	6460 & 6428
g	Waveguide short circuit	26.5-40 GHz	Mid-century Micro-wave MC 22/12
h	Ferrite isolator	26.5-40 GHz isolation >20 dBs VSWR <1.2:1	Trak Microwave Corp. 2571-1810

Initial setting up procedure

6. With the three channels of the 6500 Automatic Amplitude Analyser free of detectors, connect the 6514 under test to channel A. With the RF source switched off carry out the AUTO ZERO function pressing SHIFT and ZERO keys. A status message displayed on the screen should then read

"Ready" for channel A

and "No probe" for channels B and R

No error message should be present.

7. If an error message is present, repeat the test with the 6514 connected in turn to channels B and R to ensure that the fault is confined to the detector under test. The Auto Zero status message displayed should indicate the same fault regardless of channel.

Power accuracy (to be measured at 22° ±2°C)

Test equipment: items a,b,c,d,e,f

8. Connect an RF source capable of producing a levelled output of 0 dBm at 33 GHz, via a variable attenuator, to a high directivity directional coupler as shown in Fig. 1 below. A 6514/6500 or another power head/meter combination can be used as the monitor on the side arm of the directional coupler.

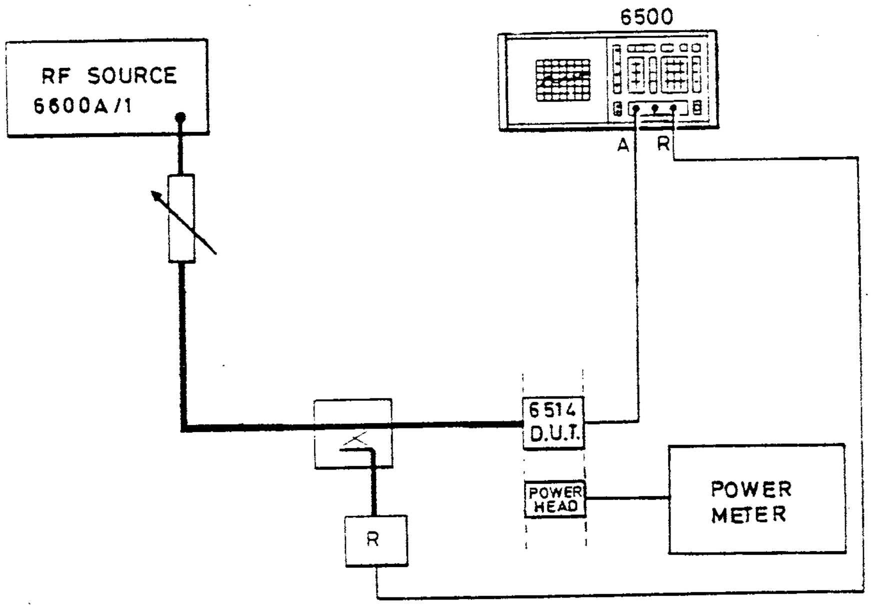


Fig. 1 Power accuracy measurement, interconnecting diagram

9. Connect the 6514 under test to channel A of the 6500 and enter the detector type information by pressing SHIFT, DET, 4 and ENTER keys. Attach the power head to the directional coupler and carry out the following steps:-

(1) With no r.f. power supplied; zero the 6514 under test and also the monitor and power head.

(2) Then with r.f. supplied at 33 GHz adjust the variable attenuator until the power meter reads 0 dBm and note the power reading on the monitor.

(3) Taking care not to handle the detector case, replace the power head with 6514 under test.

(4) Adjust the variable attenuator until the monitor power reading returns to the previous value. Allow the detector to stabilize to ambient temperature ensuring it is not in the air flow of an instrument cooling system or other thermally unstable environment. The 6500 should give a reading of 0.0 ±0.4 dBm.

VSWR confidence check

Test equipment: items a,b,c,e,g,h

10. A v.s.w.r. reading of the 6514 can be obtained by reference to Chap. 3-2, paras. 16 and 17 of the Operating Manual Vol. 1. Connections should be made as shown in Fig. 2 below, and not as illustrated in Vol. 1 Chap. 3-2, Fig. 8. There, detector A is connected so that a transmission loss measurement can also be carried out. VSWR should be better than 2.5:1.

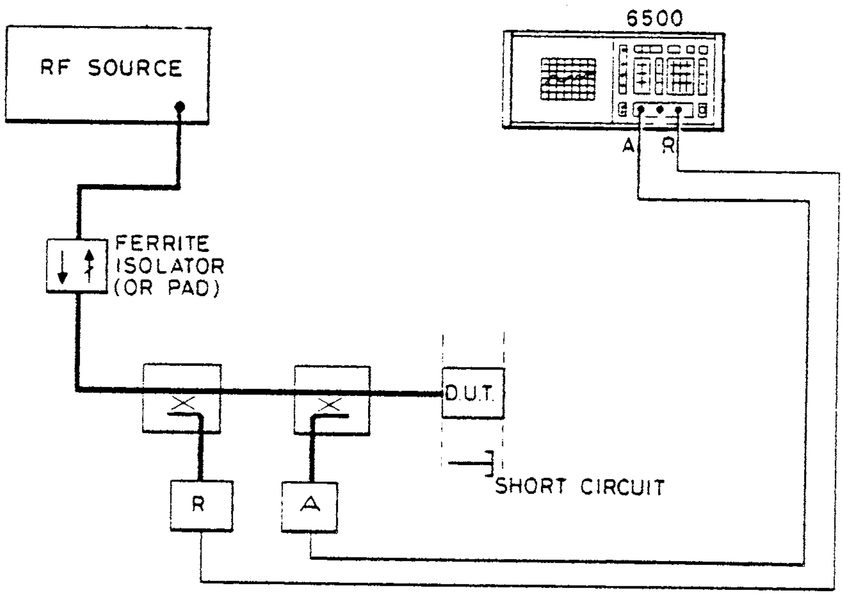


Fig. 2 VSWR measurement, interconnecting diagram

Chapter 6

REPLACEABLE PARTS

CONTENTS

INTRODUCTION

1. Each sub-assembly or printed circuit board in this equipment has been allocated a reference designator code, e.g. AC01, AC02, AC11 etc.

2. The complete component reference includes its reference designator as a prefix e.g. AC01 C1 (capacitor C1 on printed circuit board AC01) but for convenience in the text and diagrams the prefix is omitted unless it is needed to avoid confusion. However, when ordering replacements or in correspondence the complete component reference must be quoted.

ABBREVIATIONS

3. Electrical components are listed in alpha-numerical order of their complete circuit reference and the following standard abbreviations are used:

ADC	analogue-digital converter
AX	axial
CAP	capacitor
CARR	carrier
CARB	carbon
CC	carbon composition
CDE CNV	code converter
CER	ceramic
CERM	cermet
CF	carbon film
COAX	coaxial
CON	connector
CTR	counter
DAC	digital-analogue converter
DEC/DMX	decoder/demultiplexer
DECOD	decoder
DIL	dual in-line
DIV	divider
DRIV	driver
ELEC	electrolytic
ENCOD	encoder
FEM	female
FF	flip-flop (bistable)
FILTERCON	filtering capacitor
GER	germanium
GP	general purpose
ICA	integrated circuit, analogue
ICD	integrated circuit, digital
IND	inductor
INV	inverter
LD/T	lead through
MF	metal film
MG	metal glaze
MISC	miscellaneous
MO	metal oxide
MP	microprocessor
MP SUPP	microprocessor support
MUX	multiplexer
NET	network
PC	polycarbonate
PETP	(polyester)polyethelene terephthalate
PS	polystyrene
PLL	phase-locked loop

Q/ACT	quick acting
RECT	rectifier
RES	resistor
RV	resistor, variable
RX	receiver
SAPPH	sapphire
SEC	secondary
SCHM	Schmitt
SH REG	shift register
SIL	silicon
SW	switch
T/LAG	time lag
TANT	tantalum
TOG	toggle
TRANS	transistor
TX	transmitter
VAR	variable
VREG	voltage regulator
W	watts at 70°C
WW	wirewound
X	miscellaneous item
XL	crystal
!	static sensitive component
% +	asymmetric tolerance
≠	programmed EPROM

COMPONENT VALUES

4. One or more of the components fitted in the equipment may differ from those listed in this chapter for any of the following reasons:

(a) Components indicated by an * have their values selected during test to achieve particular performance limits.

(b) Owing to supply difficulties, components of different value or type may be substituted provided the overall performance of the equipment is maintained.

(c) As part of a policy of continuous development, components may be changed in value or type to obtain detail improvements in performance.

5. When there is a difference between the component fitted and the one listed, always use as a replacement the same type and value as found in the equipment. While equivalent alternatives to some components may be included during manufacture, Marconi Instruments Ltd., Microwave Products Division, should be consulted before any other alternatives are fitted when the equipment is being serviced.

ORDERING

6. When ordering replacements, address the order to our Technical Services Department (address on rear cover) or nearest agent and specify the following for each component required:-

(1) Type# and serial number of equipment

(2) Complete circuit reference

(3) Description

(4) Part number

As given on the serial number label at the rear of the equipment; if this is superseded by a model number label, quote the model number instead of the type number. Or contact your local Marconi Instruments, Microwave Products Division representative.

≠ To order a replacement programmed EPROM, specify the serial number of the instrument, and the part number of the IC required. Also specify the EPROM version number, this is identified on the IC following the part number e.g. AC01,IC6, 3964-700 Iss. 1, or 3964-700 Iss. 2.

Circuit reference	Description	Mfr./Part Number

ELECTRICAL COMPONENTS

Unit GA - General assembly

7. When ordering, prefix circuit reference with GA

Circuit reference	Description	Mfr./Part Number
	CRT NEC	190 FB31 E7-91
	MAGNET TBX15 3 MM CRT CORRECTOR	28238-157M
	YOKE & CABLE ASSY	3964-046
	GASKET	37590-742K
	SUPPORT ASSY	3964-122
	STRAP ASSY	41700-381T
	CABLE ASSY (AF03/1-AC12)	3964-040
	CABLE ASSY (AC09/2-AR04/1)	3964-279
	CABLE ASSY (AR06-AM01)	3964-042
	CABLE ASSY (AM01-AF04-AT01)	3964-043
	CABLE ASSY (AF02-AM01)	3964-044
	CABLE ASSY (MOTOR & CABLE)	3964-045
	CABLE ASSY (AF03/1-AM01)	3964-047
	FAN INST 115V 50/60 Hz 1PH 80 mm	PAPST MOTORS (8500N)
	MOTOR 12V DC	23535-401M
	I/O PANEL ASSY	3964-278
	AR04/1 PCB ASSY	3964-127
	I/O PANEL DET. ASSY	3964-274
	COAXIAL CABLE ASSY	3964-280/A,B
	GROMMET BLIND 9.52 PVC	23188-251M
	CONN RF BNC SKT FIXED (INS)	23443-449Y

Unit AC01 - Timing circuit -

8. When ordering, prefix circuit reference with AC01

Circuit reference	Description	Mfr./Part Number
	Complete unit	3964-081
C1	CAP CER .001UF 63V 10%	26383-585M
C2	CAP CER .01UF 25V 20%	26383-006C
C3	CAP CER 220PF 63V 10%	26383-587R
C4	CAP CER .01UF 25V 20%	26383-006C
C5	CAP CER .01UF 25V 20%	26383-006C
C6	CAP CER .01UF 25V 20%	26383-006C
C7	CAP CER .01UF 25V 20%	26383-006C
C8	CAP CER .01UF 25V 20%	26383-006C
C9	CAP CER .01UF 25V 20%	26383-006C
C11	CAP TANT 47UF 6V 20%	26486-232
C12	CAP CER 220PF 100V 10%	MULLARD CN15A 221K
C13	CAP TANT 10UF 35V 20%	26486-225C
C14	CAP CER .01UF 25V 20%	26383-006C
C15	CAP TANT 1.0UF 35V 20%	26486-209F
D1	DIODE SIL IN4148 100V	28336-676Ji

Circuit reference	Description	Mfr./Part Number
IC1	ICD SCHM 74LS132	28469-205N
IC2	ICD DIV 74LS90	28464-014S
IC3	ICD FF D 74LS74 DUAL+EDG TR	28462-611A
IC4	ICD DIV 74LS93	28464-117W
IC5	ICD DIV 74LS93	28464-117W
≠IC6	ICD B2716 (LINE TIMING CONTROL PROM) !	3964-700
IC7	ICD FF D 74LS273 OCT+EDG TR	28462-615U
IC8	ICD CTR 4040 !	28464-108L
≠IC9	ICD B2716 (FRAME TIMING CONTROL PROM)!	3964-701
IC10	ICD FFD 74LS273 OCT+EDG TR	28462-615U
IC11	ICD MONO 4528 !	28468-308R
IC13	ICD NAND 74LS00 QUAD 2 1NP	28466-345H
IC16	ICD NAND 74LS00 QUAD 2 1NP	28466-345H
IC17	ICD INV 74LS04	28469-171L
IC18	ICA VREG+MC78L05CP 5V OA1	MOTOROLA UA78/ TEXASL05CLP
R1	RES MF 4K7 1/4W 2%	24773-289W
R2	RES MF 2K7 1/4W 2%	24773-283L
R3	RES MF 1K0 1/4W 2%	24773-273A
R4	RES MF 1K0 1/4 2%	24773-273A
R5	RES MF 1K0 1/4W 2%	24773-273A
R6	RV CERM 50K LIN .3W 10% FLAT	25748-509C
R7	RES MF 10K 1/4W 2%	24773-297M
R8	RV CERM 50K LIN .3W 10% FLAT	25748-509C
R9	RES MF 47K 1/4W 2%	24773-313H
R10	RES MF 220R 1/4W 2%	24773-257W
R11	RV CERM 200R LIN .3W 10% FLAT	25748-502S
SKT	LOW PROFILE DIL 24	28488-044N
S1 SW	DIL 35W	23465-894E

Unit AC02/AC03 - Line generators A/B -

9. When ordering, prefix circuit reference with AC02 or AC03

	Complete unit AC02	3964-082
	Complete unit AC03	3964-083
C1	CAP CER .001UF 63V 10%	26383-585M
C2	CAP CER .001UF 63V 10%	26383-585M
C3	CAP TANT 10UF 35V 20%	26486-225C
C4	CAP CER 100PF 63V 2%	26343-477V
C5	CAP CER 100PF 63V 2%	26343-477V

Circuit reference	Description	Mfr./Part Number
Unit AC02/AC03 - Line generators A/B - (continued)		
C6	CAP CER 22PF 63V 5%	26343-469N
C8	CAP TANT 47UF 6V 20%	26486-232A
C9	CAP CER .01UF 25V 20%	26383-006C
C10	CAP CER .01UF 25V 20%	26383-006C
C11	CAP CER .01UF 25V 20%	26383-006C
C13	CAP CER .01UF 25V 20%	26383-006C
C14	CAP CER .01UF 25V 20%	26383-006C
C15	CAP CER .01UF 25V 20%	26383-006C
C16	CAP CER .01UF 25V 20%	26383-006C
C17	CAP CER .01UF 25V 20%	26383-006C
C18	CAP CER .01UF 25V 20%	26383-006C
D1	DIODE SIL 1N4148 100V	28336-676J
D2	DIODE SIL 1N4148 100V	28336-676J
IC1	ICD NAND 74LS00 QUAD 2 INP	28466-345H
IC2	ICD DEC/MUX 74LS138 3-8	28465-027F
IC3	ICD MUX 74LS157 QUAD 2 INP	28469-707B
IC4	ICD BUFF 74LS245 OCT TX RX	28469-188B
IC5	ICD MONO 74LS123 DUAL RETR	28468-309B
IC6	ICD MUX 74LS157 QUAD 2 INP	28469-707B
IC7	ICD MUX 74LS157 QUAD 2 INP	28469-707B
IC8	ICD DIV 4040 12 STAGE	28464-108L
IC9	ICD RAM 2114AL-4 1Kx4 BIT 200NS !	28469-306Y
IC10	ICD RAM 2114AL-4 1Kx4 BIT 200NS !	28469-306Y
IC13	ICD CTR 74LS197 4 BIT BIN PRE	28464-116S
IC14	ICD CTR 74LS197 4 BIT BIN PRE	28464-116S
IC15	ICD CTR 74LS197 4 BIT BIN PRE	28464-116S
IC16	ICD CTR 74LS197 4 BIT BIN PRE	28464-116S
IC17	ICD NAND 74LS00 QUAD 2 INP	28466-345H

Circuit reference	Description	Mfr./Part Number

Unit AC02/AC03 - Line generators A/B - (continued)

IC18	ICD FFD 74LS74 DUAL+EDG TR	28462-611A
IC19	ICD FFD 74LS74 DUAL+EDG TR	28462-611A
IC20	ICD OR 74LS32 QUAD 2 1NP	28466-108U
IC21	ICD MONO 74LS123 DUAL RETR	28468-309B
IC22	ICD NAND 74LS00 QUAD 2 1NP	28466-345H
IC23	ICD OR 74LS32 QUAD 2 1NP	28466-108U
R1	RES RV CERM 10K LIN .3W 10% FLAT	25748-507X
R2	RES MF 5K6 1/4W 2%	24773-291S
R3	RES RV CERM 10K LIN .3W 10% FLAT	25748-507X
R4	RES MF 5K6 1/4W 2%	24773-291S
R5	RES MF 4K7 1/4W 2%	24773-289W
R6	RES MF 4K7 1/4W 2%	24773-289W
R7	RES MF 1K0 1/4W 2%	24773-273A
R8	RES MF 1K0 1/4W 2%	24773-273A
R9	RES MF 15K 1/4W 2%	24773-301P

Unit AC04/1 - Video circuit (graticule)

10. When ordering, prefix circuit reference with AC04/1

	Complete unit	3964-139
C1	CAP CER .01UF 25V 20%	26383-006C
C2	CAP CER .01UF 25V 20%	26383-006C
C3	CAP CER .01UF 25V 20%	26383-006C
C4	CAP CER .01UF 25V 20%	26383-006C
C5	CAP CER .01UF 25V 20%	26383-006C
C6	CAP CER .01UF 25V 20%	26383-006C
C7	CAP CER .01UF 25V 20%	26383-006C
C8	CAP CER .01UF 25V 20%	26383-006C
C9	CAP CER .01UF 25V 20%	26383-006C
C10	CAP CER .01UF 25V 20%	26383-006C
C11	CAP CER .01UF 25V 20%	26383-006C
C12	CAP CER .01UF 25V 20%	26383-006C
C13	CAP CER .01UF 25V 20%	26383-006C
C14	CAP CER .01UF 25V 20%	26383-006C
C15	CAP CER .01UF 25V 20%	26383-006C

Circuit reference	Description	Mfr./Part number
Unit AC04/1 - Video circuit (graticule) - (continued)		
C16	CAP CER 100PF 6.3V 2%	26343-477V
C17	CAP CER .001UF 63V 10%	26383-585M
C19	CAP TANT 47UF 6V 20%	26486-232A
D1	DIODE SIL 1N4148 100V	28336-676J
D2	DIODE SIL 1N4148 100V	28336-676J
D3	DIODE SIL 1N4148 100V	28336-676J
D4	DIODE SIL 1N4148 100V	28336-676J
D5	DIODE SIL 1N4148 100V	28336-676J
D6	DIODE SIL 1N4148 100V	28336-676J
IC1	ICD BUFF 74LS244 OCT 3 ST	28469-182T
IC2	ICD DEC/DMX 74LS138 3-8	28465-027F
IC3	ICD DEC/DMX 74LS138 3-8	28465-027F
IC4	ICD OR 74LS32 QUAD 2 INP	28466-108U
IC5	ICD DIV 4040 12 STAGE !	28464-108L
IC6	ICD MUX 74LS157 QUAD 2 INP	28469-707B
IC7	ICD BUFF 74LS244 OCT 3 ST	28469-182T
IC8	ICD RAM 2114 AL-4 1Kx4BIT 200NS !	28469-306Y
IC9	ICD MONO 74LS123 DUAL RETR	28468-309B
IC10	ICD MUX 74LS157 QUAD 2 INP	28469-707B
IC11	ICD NAND 74LS00 QUAD 2 INP	28466-345H
IC12	ICD FF D 74LS273 OCT+EDG TR	28462-615U
IC13	ICD NAND 74LS00 QUAD 2 INP	28466-345H
IC14	ICD NAND 74LS10 TRIP 3 INP	28466-351Y
IC15	ICD NAND 74LS00 QUAD 2 INP	28466-345H
R1	RES MF 4K7 1/4W 2%	24773-289W
R2	RES MF 1K0 1/4W 2%	24773-273A
R3	RES MF 4K7 1/4W 2%	24773-289W
R4	RES MF 4K7 1/4W 2%	24773-289W
R5	RV CERM 1K LIN .3W 10% FLAT	25748-504D
R6	RV CERM 1K LIN .3W 10% FLAT	25748-504D
R7	RV CERM 1K LIN .3W 10% FLAT	25748-504D
R8	RV CERM 1K LIN .3W 10% FLAT	25748-504D
R9	RV CERM 1K LIN .3W 10% FLAT	25748-504D
R10	RV CERM 1K LIN .3W 10% FLAT	25748-504D

Circuit reference	Description	Mfr./Part number
Unit AC04/1 - Video circuit (graticule) - (continued)		
R11	RES MF 470R 1/4W 2%	24773-265M
R12	RES MF 470R 1/4W 2%	24773-265M
R13	RES MF 470R 1/4W 2%	24773-265M
R14	RES MF 470R 1/4W 2%	24773-265M
R15	RES MF 470R 1/4W 2%	24773-265M
R16	RES MF 470R 1/4W 2%	24773-265M
R17	RES MF 1K0 1/4W 2%	24773-273A
R18	RES MF 1K0 1/4W 2%	24773-273A
R19	RES MF 1K0 1/4W 2%	24773-273A
R20	RES MF 270R 1/4W 2%	244773-259T
R21	RES MF 1K0 1/4W 2%	24773-273A
R22	RES MF 22R 1/4W 2%	24773-233M
R23	RES MF 3K3 1/4W 2%	24773-285F
R24	RES MF 690R 1/4W 2%	24773-269K
TR1	NSI 2N2369 500M-SW	28452-771P
TR2	BC308B	28433-455R
TR3	BC308B	28433-455R

Unit AC05 - Alpha generator -

11. When ordering, prefix circuit reference with AC05

Circuit reference	Description	Mfr./Part number
	Complete unit	3964-085
C2	CAP PS 100P 350V 2PF AX	26516-243J
C3	CAP PS 100P 350V 2PF AX	26516-243J
C4	CAP TANT 47UF 6V 20%	26486-232A
C5	CAP CER .01UF 25V 20%	26383-006C
C6	CAP CER .01UF 25V 20%	26383-006C
C7	CAP CER .01UF 25V 20%	26383-006C
C8	CAP CER .01UF 25V 20%	26383-006C
C9	CAP CER .01UF 25V 20%	26383-006C
C10	CAP CER .01UF 25V 20%	26383-006C
C11	CAP CER .01UF 25V 20%	26383-006C
C12	CAP CER .01UF 25V 20%	26383-006C
C13	CAP CER .01UF 25V 20%	26383-006C
C14	CAP CER .01UF 25V 20%	26383-006C
C15	CAP CER .01UF 25V 20%	26383-006C

Circuit reference	Description	Mfr./Part Number
Unit AC05 - Alpha generator - (continued)		
C16	CAP CER .01UF 25V 20%	26383-006C
C17	CAP CER .01UF 25V 20%	26383-006C
C18	CAP CER .01UF 25V 20%	26383-006C
IC1	ICD DEC/DMX 74LS138 3-8	28465-027F
IC2	ICD FF JK 4027 DUAL B1 !	28462-018C
IC3	ICD FF JK 4027 DUAL B1 !	28462-018C
IC4	ICD BUFF 74LS244 OCT 3 STATE	28469-182T
IC5	ICD NOR 74LS02 QUAD 2 INP	28466-214Y
IC6	ICD RAM 2114 AL-4 1Kx4BIT 200NS !	28469-306Y
IC7	ICD RAM 2114 AL-4 1Kx4BIT 200NS !	28469-306Y
IC8	ICD MUX 74LS157 QUAD 2 INP	28469-707B
IC9	ICD MUX 74LS157 QUAD 2 INP	28469-707B
IC10	ICD MUX 74LS157 QUAD 2 INP	28469-707B
IC11	ICD CTR 74LS197 4BIT BIN PRE	28464-116S
IC12	ICD CTR 74LS197 4BIT BIN PRE	28464-116S
IC13	ICD CTR 74LS197 4BIT BIN PRE	28464-116S
IC14	ICD LATCH 74LS75 QUAD	28462-408U
IC15	ICD LATCH 74LS75 QUAD	28462-408U
IC16	ICD LATCH 74LS75 QUAD	28462-408U
≠IC17	ICD B2716 (ALPHANUMERIC CHAR.GEN.PROM) !	3964-702
IC18	ICD SH REG 74LS165 8BIT PISO	TEXAS OR MOTOROLA SN 74LS165N
IC20	ICD MONO 74LS123 DUAL RETR	28468-309B
IC21	ICD NAND 74LS00 QUAD 2 INP	28466-345H
IC22	ICD FF D 74LS74 DUAL+EDG TR	28462-611A
IC23	ICD DIV 4040 12 STAGE !	28464-108L
R1	RES MF 100K 1/4W 2%	24773-321L
R2	RES MF 10K 1/4W 2%	24773-297M
R3	RES MF 3K9 1/4W 2%	24773-287V
SKT	LOW PROFILE DIL 24	28488-044N

Circuit reference	Description	Mfr./Part Number

Unit AC18 - Microprocessor -

12. When ordering, prefix circuit reference with AC18

	Complete unit	3964-079
C1	CAP TANT 47UF 6V 20%	26486-232A
C2	CAP TANT 1UF 35V 20%	26486-209F
C3	CAP CER .1UF 50V 20%	26383-534Y
C4	CAP CER .1UF 50V 20%	26383-534Y
C5	CAP CER .1UF 50V 20%	26383-534Y
C6	CAP CER .1UF 50V 20%	26383-534Y
C7	CAP CER .1UF 50V 20%	26383-534Y
C8	CAP TANT 1UF 35V 20%	26486-209F
C9	CAP TANT 1UF 35V 20%	26486-209F
C10	CAP CER .1UF 50V 20%	26383-534Y
C11	CAP TANT 1UF 35V 20%	26486-209F
C12	CAP TANT 1UF 35V 20%	26486-209F
C13	CAP CER .1UF 50V 20%	26383-534Y
C14	CAP CER .1UF 50V 20%	26383-534Y
C15	CAP CER .1UF 50V 20%	26383-534Y
C16	CAP CER .1UF 50V 20%	26383-534Y
C17	CAP CER .1UF 50V 20%	26383-534Y
C18	CAP CER .1UF 50V 20%	26383-534Y
C19	CAP CER .1UF 50V 20%	26383-534Y
C20	CAP CER .1UF 50V 20%	26383-534Y
C21	CAP CER .1UF 50V 20%	26383-534Y
C22	CAP TANT 47UF 6V 20%	26486-232A
C23	CAP TANT 1UF 35V 20%	26486-209F
CON.	JUMP FEM 2 1 ROW (LINKS 1,2,3 & 4)	23435-990X
D1	DIODE SIL 4148 100V	28336-676J
IC1	ICD MP 8085A-2 8 BIT NMOS !	28469-415F
IC2	ICD INV 74LS04 HEX	28469-171L
IC3	ICD DEC/DMX 74LS139 DUAL 2-4	28469-029V
IC4	ICD NAND 74LS00 QUAD 2 INP	28466-345H
IC5	ICD DEC/DMX 74LS138 3-8	28465-027F
IC6	ICD DEC/DMX 74LS138 3-8	28465-027F
#IC7	ICD 2764 (CONTROL PROM PT.1) !	3964-715
#IC8	ICD 2764 (CONTROL PROM PT.2) !	3964-716
#IC9	ICD 2764 (CONTROL PROM PT.3) !	3964-717
#IC10	ICD 2764 (CONTROL PROM PT.4) !	3964-718

Circuit reference	Description	Mfr./Part Number
Unit AC18 - Microprocessor (continued)		
IC11	ICD BUFF 74LS245 OCT TX RX	28469-188B
IC12	ICD FF D 74LS74 DUAL+EDG TR	28462-611A
IC13	ICD FF D 74LS74 DUAL+EDG TR	28462-611A
IC14	ICD BUFF 74LS244 OCT 3 ST	28469-182T
IC15	ICD LATCH 74LS373 OCT 3 ST	28462-410E
IC16	ICD BUFF 74LS244 OCT 3 ST	28469-182T
IC17	ICD RAM HM6116P-4 2Kx8 BIT 200NS !	28469-307N
IC18	ICD RAM HM6116P-4 2Kx8 BIT 200NS !	28469-307N
IC19	ICD RAM HM6116P-4 2Kx8 BIT 200NS !	28469-307N
IC20	ICD RAM HM6116P-4 2Kx8 BIT 200NS !	28469-307N
IC21	ICD AND 74LS08 QUAD 2 INP	28466-012L
R1	RES MF 10K 1/4W 2%	24773-297M
R2	RES MF 10K 1/4W 2%	24773-297M
R3	RES MF 10K 1/4W 2%	24773-297M
R4	RES MF 10K 1/4W 2%	24773-297M
R5	RES MF 1K 1/4W 2%	24773-273A
R6	RES MF 150R 1/4W 2%	24773-253F
R7	RES MF 1K 1/4W 2%	24773-273A
R9	RES MF 1K 1/4W 2%	24773-273A
SKT	LOW PROFILE DIL 28	28488-045L
XL1	10 MHz CRYSTAL	28312-047U

Unit AC09/2 - In-Out (Port control)

13. When ordering, prefix circuit reference with AC09/2

	Complete unit	3964-135
C1	CAP CER .1UF 50V 20%	26383-534Y
C2	CAP CER .1UF 50V 20%	26383-534Y
C3	CAP CER .1UF 50V 20%	26383-534Y
C4	CAP CER 330P 63V 2%	26343-483DOx
C5	CAP TANT 10UF 35V 20%	26486-225C
C6	CAP TANT 47UF 6V 20%	26486-232A
C7	CAP TANT 10UF 35V 20%	26486-225C
C8	CAP CER .1UF 50V 20%	26383-534Y
C9	CAP CER .1UF 50V 20%	26383-534Y
C10	CAP CER .1UF 50V 20%	26383-534Y
C11	CAP CER .1UF 50V 20%	26383-534Y
C12	CAP PETP .22UF 100V 10%	26582-226G
C13	CAP TANT .47UF 35V 20%	26486-207L
C14	CAP CER .1UF 50V 20%	26383-534Y
C15	CAP CER .1UF 50V 20%	26383-534Y

Circuit reference	Description	Mfr./Part Number
Unit AC09/2 - In-Out (Port control) - (continued)		
C16	CAP PETP .22UF 100V 10%	26582-226G
C17	CAP TANT .47UF 35V 20%	26486-207L
C18	CAP CER .01UF 25V 20%	26383-006C
C19	CAP TANT 1UF 35V 20%	26486-209F
C20	CAP CER .01UF 25V 20%	26383-006C
C21	CAP TANT 1UF 35V 20%	26486-209F
C22	CAP TANT 1UF 35V 20%	26486-209F
C23	CAP CER .01UF 25V 20%	26383-006C
C24	CAP TANT 1UF 35V 20%	26486-209F
C25	CAP CER .01UF 25V 20%	26383-006C
C26	CAP TANT 4.7UF 35V 20%	26486-219P
C27	CAP CER .01UF 25V 20%	26383-006C
C28	CAP TANT 1UF 35V 20%	26486-209F
C29	CAP CER .1UF 50V 20%	26383-534Y
C30	CAP CER 100PF 63V 2%	26343-477V
C31	CAP CER .01UF 25V 20%	26383-006C
C32	CAP TANT 1UF 35V 20%	26486-209F
C33	CAP TANT 1UF 35V 20%	26486-209F
C34	CAP CER .01UF 25V 20%	26383-006C
C35	CAP CER .1UF 50V 20%	26383-534Y
C36	CAP CER .01UF 25V 20%	26383-006C
C37	CAP TANT 1UF 35V 20%	26486-209F
C38	CAP CER 100PF 63V 2%	26343-477V
C39	CAP TANT 1UF 35V 20%	26486-209F
C40	CAP CER .01UF 25V 20%	26383-006C
C41	CAP CER .01UF 25V 20%	26383-006C
C42.	CAP TANT 1UF 35V 20%	26486-209F
C43	CAP TANT 1UF 35V 20%	26486-209F
C44	CAP CER .01UF 25V 20%	26383-006C
C45	CAP CER .01UF 25V 20%	26383-006C
C46	CAP TANT 1UF 35V 20%	26486-209F
C47	CAP CER .01UF 25V 20%	26383-006C
C48	CAP CER .001UF 63V 10%	26383-242P
C49	CAP CER .001UF 63V 10%	26383-242P
C50	CAP CER .01UF 25V 20%	26383-006C
C51	CAP TANT 1UF 35V 20%	26486-209F
D1	DIODE SIL 1N4148 100V	28336-676J
D4	DIODE ZENER 1N829 6.2 V 5%	28371-530K
D5	DIODE SIL 1N4148 100V	28336-676J

Circuit reference	Description	Mfr./Part Number
Unit AC09/2 - In-Out (Port control) - (continued)		
IC1	ICD BUFF 74LS125A QUAD 3ST	28469-184X
IC2	ICD DEC/MUX 74LS138 3-8	28465-027F
IC3	ICD NAND 74LS00 QUAD 2 INP	28466-345H
IC4	ICD NAND 74LS00 QUAD 2 INP	28466-345H
IC5	ICD FF D 74LS273 OCT+EDG TR	28462-615U
IC6	ICD FF D 74LS273 OCT+EDG TR	28462-615U
IC7	ICA ADC ZN425E 8-BIT DAC/ADC	28469-381G
IC8	ICA AMP TL072CP DUAL FET 1/P	28461-348Z
IC9	ICD FFD 74LS273 OCT+EDG TR	28462-615U
IC10	ICA ADC ZN425E - 8BIT DAC/ADC	28469-381G
IC11	ICA AMP TL072CP DUAL FET	28461-348Z
IC12	ICA DAC AD7542 KN !	ANALOG DEVICES SINGLE SOURCE
IC13	ICA AMP OP-07CP 150UV O/S DIL8	28461-374M
IC14	ICA DAC AD7542 KN!	ANALOG DEVICES SINGLE SOURCE
IC15	ICA AMP OP-07C 150UV O/S DIL8	28461-374U
IC16	ICA (ARRAY) CA3046	28461-901A
IC17	ICA LM311N	28461-695U
IC18	ICA AMP TL072CP DUAL FET I/P	28461-348Z
PL1	MALE 50 PCB ELBOW CONN SMB	23444-359Z
PL2	MALE 50 PCB ELBOW CONN SMA	23444-359Z
PL3	G08D10A 9 BEBA-C CONN PCB	ITT CANNON
R1	RES MF 1K 1/4W 2%	24773-273A
R2	RES MF 1K 1/4W 2%	24773-273A
R3	RES MF 100K 1/4W 2%	24773-321L
R4	RES MF 20K 1/4W 2%	24773-304C
R5	RES MF 10K 1/4W 2%	24773-297M
R6	RES MF 200K 1/4W 2%	24773-328D
R7	RES MF 10K 1/4W 2%	24773-297M
R8	RES MF 27K 1/4W 2%	24773-307K
R9	RES MF 4K7 1/4W 2%	24773-506P
R10	RES MF 4K7 1/4W 2%	24773-289W
R11	RES MF 5K6 1/4W 2%	24773-291S
R12	RV CERM 5K LIN 10%	25748-506P
R13	RES MF 1K2 1/4W 2%	24773-275H
R14	RES MF 18K 1/4W 2%	24773-303M
R15	RES MF 220R 1/4W 2%	24773-257W

Circuit reference	Description	Mfr./Part Number
Unit AC09/2 - In-Out (Port control) - (continued)		
R16	RES MF 10K 1/4W 2%	24773-297M
R17	RES MF 4K7 1/4W 2%	24773-289W
R18	RES MF 220R 1/4W 2%	24773-257W
R19	RES MF 1K 1/4W 2%	24773-273A
R20	RES MF 2K2 1/4W 2%	24773-281Y
R21	RES MF 10K 1/4W 2%	24773-297M
R22	RES MF 10K 1/4W 2%	24773-297M
R23	RES MF 47K 1/4W 2%	24773-313H
R24	RES MF 27K 1/4W 2%	24773-307K
R25	RES MF 10K 1/4W 2%	24773-297M
R26	RES MF 10K 1/4W 2%	24773-297M
R27	RES MF 4K7 1/4W 2%	24773-289W
R28	RES MF 4K7 1/4W 2%	24773-289W
R29	RES MF 4K7 1/4W 2%	24773-289W
R30	RES MF 4K7 1/4W 2%	24773-289W
R31	RES MF 4K7 1/4W 2%	24773-289W
R32	RES MF 4K7 1/4W 2%	24773-289W
R33	RES MF 4K7 1/4W 2%	24773-289W
R34	RES MF 100R 1/4W 2%	24773-249J
R35	RES MF 150K 1/4W 2%	24773-825V
R36	RES MF 1M 1/4W 2%	24773-346E
R37	RES MF 100R 1/4W 2%	24773-249J
R38	RES MF 100K 1/4W 2%	24773-321L
R39	RES MF 100K 1/4W 2%	24773-321L
R40	RES MF 33K 1/4W 2%	24773-309Z
R41	RES MF 10K 1/4W 2%	24773-297M
R42	RES MF 100K 1/4W 2%	24773-321L
R43	RES MF 15K 1/4W 2%	24773-301P
R44	RES MF 4K7 1/4W 2%	24773-289W
R45	RES MF 4K7 1/4W 2%	24773-289W
R46	RES MF 820R 1/4W 2%	24773-271B
SKT	LOW PROFILE DIL 16	28488-041E
TR1	TR NS1 2N2369 15V 500M-SW	28452-197H
TR2		TEXAS TIP 120 OR RCA 2N6387
TR3	TR NS1 2N2369 15V 500M-SW	28452-197H
TR4	TR NS1 2N2369 15V 500M-SW	28452-197H

Circuit reference	Description	Mfr./Part Number

Unit AC11 - A-D system and log conversion -

14. When ordering, prefix circuit reference with AC11

	Complete unit	3964-091
C4	CAP TANT 1.0UF 35V 20%	26486-209F
C5	CAP CER .01UF 25V 20%	26383-006C
C8	CAP TANT 10UF 35V 20%	26486-225C
C9	CAP TANT 10UF 35V 20%	26486-225C
C11	CAP TANT 10UF 35V 20%	26486-225C
C12	CAP TANT 10UF 35V 20%	26486-225C
C13	CAP TANT 10UF 35V 20%	26486-225C
C14	CAP CER .01UF 25V 20%	26383-006C
C15	CAP CER .01UF 25V 20%	26383-006C
C16	CAP CER .01UF 25V 20%	26383-006C
C17	CAP CER .01UF 25V 20%	26383-006C
C18	CAP CER .01UF 25V 20%	26383-006C
C19	CAP CER .01UF 25V 20%	26383-006C
C20	CAP CER .01UF 25V 20%	26383-006C
C21	CAP CER .01UF 25V 20%	26383-006C
C22	CAP CER .01UF 25V 20%	26383-006C
C23	CAP CER .01UF 25V 20%	26383-006C
C24	CAP CER .01UF 25V 20%	26383-006C
IC3	ICA ADC 80-12 !	ANALOG DEV. SINGLE SOURCE
IC4	ICD AND/OR 4019 QUAD SELECT B1	28466-452U
IC5	ICD AND/OR 4019 QUAD SELECT B1	28466-452U
IC6	ICD AND/OR 4019 QUAD SELECT B1	28466-452U
IC7	ICD COMP 4585 4 BIT !	28469-384W
IC8	ICD COMP 4585 4 BIT !	28469-384W
IC9	ICD COMP 4585 4 BIT !	28469-384W
IC10	ICD NAND 4011 QUAD 2 INP B1	28466-340R
IC11	ICD OR 4072 DUAL 4 INP !	28466-106H
IC12	ICD OR 4071 QUAD 2 INP B1	28466-403P
IC13	ICD NOR 4001 QUAD 2 INP B1 !	28466-207Z
IC14	ICD AND/OR 4019 QUAD SELECT B1	28466-452U
IC15	ICD AND/OR 4019 QUAD SELECT B1	28466-452U
IC16	ICD AND/OR 4019 QUAD SELECT B1	28466-452U
≠IC18	ICD B2716 (ADC LOG TABLE MSB PROM) !	3964-704
≠IC19	ICD B2716 (ADC LOG TABLE LSB PROM) !	3964-703
IC20	ICD DRIV 74LS367 3 STATE	TEXAS SN 74LS367AN NAT.S. DM 74LS367N
IC21	ICD FF D 74LS273 OCT+EDG TR	28462-615U
IC22	ICD DEC/DMX 74LS138 3-8	88465-027F
SKT	LOW PROFILE DIL 24	28488-044N

Circuit reference	Description	Mfr./Part Number

Unit AC12 - Signal channel -

15. When ordering, prefix circuit reference with AC12

	Complete unit	3964-092
C1	CAP PETP .22UF 100V 10%	26582-226G
C2	CAP TANT 1UF 35V 20%	26486-209F
C3	CAP TANT 1UF 35V 20%	26486-209F
C4	CAP PETP .47UF 63V 10%	26582-410P
C5	CAP PETP .022UF 250V 10%	26582-204X
C6	CAP TANT 4.7UF 35V 20%	26486-219P
C7	CAP TANT 4.7UF 35V 20%	26486-219P
C8	CAP TANT 4.7UF 35V 20%	26486-219P
C9	CAP TANT 4.7UF 35V 20%	26486-219P
C11	CAP TANT 4.7UF 35V 20%	26486-219P
C12	CAP TANT 4.7UF 35V 20%	26486-219P
C13	CAP PETP .047UF 250V 10%	26582-206C
C14	CAP PETP .047UF 250V 10%	26582-206C
C15	CAP CER .001UF 63V 20%	26383-585M
C16	CAP CER .001UF 63V 20%	26383-585M
C18	CAP CER .01UF 25V 20%	26383-006C
C22	CAP TANT 10UF 35V 20%	26486-225C
C23	CAP TANT 10UF 35V 20%	26486-225C
C25	CAP TANT 4.7UF 35V 20%	26486-219P
C26	CAP TANT 4.7UF 35V 20%	26486-219P
C29	CAP TANT 10UF 35V 20%	26486-225C
C30	CAP TANT 10UF 35V 20%	26486-225C
C31	CAP TANT 22UF 16V 20%	26486-230B
C32	CAP CER .001UF 63V 20%	26383-585M
C34	CAP CER 100PF 63V 2%	26343-477V
C36	CAP CER 100PF 63V 2%	26343-477V
C37	CAP CER 100PF 63V 2%	26343-477V
C38	CAP CER .001UF 63V 20%	26383-585M
C43	CAP CER 270PF 63V 2%	26343-482W
C44	CAP CER .1UF 50V 20%	26383-534Y
C45	CAP CER .01UF 25V 20%	26383-006C
D2	DIODE ZENER BZX79C8V2 8.2V	MULLARD
D3	DIODE ZENER BZX79C8V2 8.2V	MULLARD
D4	DIODE ZENER BZX79C8V2 8.2V	MULLARD
D5	DIODE ZENER BZX79C8V2 8.2V	MULLARD
D6	DIODE SIL 1N4148 100V	28336-676J

Circuit reference	Description	Mfr./Part number
Unit AC12 - Signal channel - (continued)		
D7	DIODE SIL 1N4148 100V	28336-676J
D8	DIODE ZENER BZX79 12V	28372-149G
D9	DIODE SIL 1N4148 100V	28336-676J
D10	DIODE SIL 1N4148 100V	28336-676J
IC1	ICA AMP OP-01CJ	BOURNS TRIMPOT OR ANALOG DEVICES
IC2	ICA SW DG200BA DUAL TO100 !	28469-362R
IC3	ICA AMP OP-01CJ	BOURNE TRIMPOT OR ANALOG DEVICES
IC4	ICA SW DG200BA DUAL TO100 !	28469-362R
IC5	ICA AMP TL072CP DUAL FET 1/P	28461-348Z
IC6	MC14538 BCP !	MOTOROLA
IC7	ICA AMP TL072CP DUAL FET 1/P	28461-348Z
IC8	ICD FF D 4013 DUAL BI !	28462-608A
IC9	ICA SW DG200BA DUAL TO100 !	28469-362R
IC10	ICA AMP TL071CP FET 1/P DIL 8	TEXAS
IC12	ICA SW DG200BA DUAL TO100 !	28469-362R
IC14	MC14538B !	MOTOROLA
IC15	ICD FF D 4013 DUAL BI !	28462-608A
IC16	ICA AMP TL071CP FET 1/P DILS	TEXAS
R1	RES MF 4K7 1/4W 2%	24773-289W
R2	RES MF 100R 1/4W 2%	24773-249J
R3	RES MF 100R 1/4W 2%	24773-249J
R4	RES MF 150K 1/4W 2%	24773-325V
R5	RV CERM 50K LIN .3W 10% FLAT	25748-509C
R6	RES MF 1K8 1/4W 2%	24773-279N
R8	RES MF 100R 1/4W 2%	24773-249J
R9	RES MF 100R 1/4W 2%	24773-249J
R10	RES MF 2K2 1/4W 2%	24773-281Y
R11	RES MF 100R 1/4W 2%	24773-249J
R12	RES MF 100R 1/4W 2%	24773-249J
R13	RES MF 27K 1/4W 2%	24773-307K
R14	RV CERM 5K LIN .3W 10% FLAT	25748-506P
R15	RES MF 3K3 1/4W 2%	24773-285F
R16	RES MF 22K 1/4W 2%	24773-305R
R17	RES MF 100R 1/4W 2%	24773-249J
R18	RES MF 100R 1/4W 2%	24773-249J
R19	RES MF 1K 1/4W 2%	24773-273A
R20	RES MF 4K7 1/4W 2%	24773-289W
R21	RES MF 1K 1/4W 2%	24773-273A

Circuit reference	Description	Mfr./Part Number
Unit AC12 - Signal channel - (continued)		
R22	RES MF 10K 1/4W 2%	24773-297M
R23	RES MF 10K 1/4W 2%	24773-297M
R24	RES MF 4K7 1/4W 2%	24773-289W
R25	RES MF 5K6 1/4W 2%	24773-291S
R26	RES MF 5K6 1/4W 2%	24773-291S
R27	RES MF 10K0 1/4W 0.5%	24753-628N
R28	RES MF 10K0 1/4W 0.5%	24753-628N
R29	RES MF 10K0 1/4W 0.5%	24753-628N
R30	RES MF 10K0 1/4W 0.5%	24753-628N
R31	RV 10K 10%	BOURNS 3299W-1-103 OR ALLEN BRADLEY - 85W/10K
R32	RV 10K 10%	BOURNS 3299W-1-103 OR ALLEN BRADLEY - 85W/10K
R33	RV CERM 2K LIN .3W 10% FLAT	25748-505T
R34	RES MF 4K7 1/4W 2%	24773-289W
R35	RES MF 10K 1/4W 2%	24773-297M
R36	RES MF 10K 1/4W 2%	24773-297M
R37	RES MF 4K7 1/4W 2%	24773-289W
R38	RES MF 10K 1/4W 2%	24773-297M
R39	RES MF 5K6 1/4W 2%	24773-291S
R40	RES MF 100R 1/4W 2%	24773-249J
R42	RES MF 22K 1/4W 2%	24773-305R
R44	RES MF 27K 1/4W 2%	24773-307K
R49	RES MF 5K6 1/4W 2%	24773-291S
R50	RV CERM 10K LIN .5W 10%	25748-566S
R51	RES MF 22K 1/4W 2%	24773-305R
R52	RES MF 15K 1/4W 2%	24773-301P
R53	RES MF 15K 1/4W 2%	24773-301P
R54	RES MF 1K8 1/4W 2%	24773-279N
R55	RES MF 1K 1/4W 2%	24773-273A
R56	RES MF 10K 1/4W 2%	24773-297M
R57	RES MF 10K 1/4W 2%	24773-297M
R58	RES MF 10K 1/4W 2%	24773-297M
R61	RV CERM 10K LIN .5W 10%	25748-566S
R62	RES MF 15K 1/4W 2%	24773-301P
R63	RES MF 4K7 1/4W 2%	24773-297M
R64	RES MF 1K 1/4W 2%	24773-273A
R65	RES MF 100R 1/4W 2%	24773-249J
R66	RES MF 100R 1/4W 2%	24773-249J
R67	RES MF 10K 1/4W 2%	24773-297M

Circuit reference	Description	Mfr./Part number

Unit AC12 - Signal channel - (continued)

R70	RES MF 1K 1/4W 2%	24773-273A
R72	RES MF 100R 1/4W 2%	24773-249J
R73	RES MF 100R 1/4W 2%	24773-249J
SK2	CON RF SMB MALE 50 PCB ELBOW	23444-359Z
TR1	TP PSI BC307A 45V 130M-GEN	28435-227H
TR2	TR PSI BC307A 45V 130M-GEN	28435-227H
TR4	TR NSI 2N2369 15V 500M-SW	28452-197H
TR5	TR NSI 2N2369 15V 500M-SW	28452-197H

Unit AF01 - Keyboard -

16. When ordering, prefix circuit reference with AF01

	Complete assy.	3964-093
	CONN. JUMP MALE FST-2.1A-10	T & B ANSLEY
D1	LAMP LED CQY87V180P 2.4V YEL	28624-121Z
D2	LAMP LED CQY87V180P 2.4V YEL	28624-121Z
S1-S39	SW PUSH ICO 24V 10MA	23465-411B

Unit AF02 - Keyboard decoder -

17. When ordering, prefix circuit reference with AF02

	Complete unit	3964-094
C1	CAP CER 39PF 63V 5%	26343-472N
C2	CAP CER .01UF 25V 20%	26383-006C
C3	CAP PETP .047UF 250V 10%	26582-206C
C4	CAP CER .01UF 25V 20%	26383-006C
C5	CAP TANT 4.7UF 35V 20%	26486-219P
C6	CAP TANT 4.7UF 35V 20%	26486-219P
C7	CAP TANT 4.7UF 35V 20%	26486-219P
C8	CAP TANT 4.7UF 35V 20%	26486-219P
C9	CAP TANT 4.7UF 35V 20%	26486-219P
C10	CAP CER .01UF 25V 20%	26383-006C

Circuit reference	Description	Mfr./Part Number
Unit AF02 - Keyboard decoder - (continued)		
C11	CAP CER .01UF 25V 20%	26383-006C
C12	CAP CER .01UF 25V 20%	26383-006C
C13	CAP CER .01UF 25V 20%	26383-006C
C14	CAP CER .01UF 25V 20%	26383-006C
C15	CAP CER .01UF 25V 20%	26383-006C
D1	DIODE SIL 1N4148 100V	28336-676J
D2	DIODE SIL 1N4148 100V	28336-676J
D3	DIODE SIL 1N4148 100V	28336-676J
D4	DIODE SIL 1N4148 100V	28336-676J
D5	DIODE SIL 1N4148 100V	28336-676J
D6	DIODE SIL 1N4148 100V	28336-676J
IC1	ICD ENCODER KR 2376 STP !	SMC VIA RASTRA
IC2	ICD FF D 4013 DUAL BI !	28462-608A
IC3	ICA AMP UA741CN GP DIL8	28461-304T
IC4	ICA AMP UA741CN GP DIL8	28461-304T
IC5	ICA AMP UA741CN GP DIL8	28461-304T
IC6	ICD BUFF 4049B HEX INV BI !	28469-162Z
IC7	ICD BUFF 4049B HEX INV BI !	28469-162Z
IC8	ICD DRIV 74LS367 3 STATE	TEXAS SN74LS367AN OR NAT.S. DM74LS367N
IC9	ICD DRIV 74LS367 3 STATE	TEXAS SN74LS367AN OR NAT.S. DM74LS367N
IC10	ICD DEC/DMX 74LS138 3-8	28465-027F
IC11	ICD FFD 74LS74 DUAL+EDG TR	28462-611A ITT STOCK NO.64121A
IC12	ICA VREG MC78L12CP	OR AERIES
IC13	ICA VREG MC78L12CP	MOTOROLA
R1	RES MF 100K 1/4W 2%	24773-321L
R2	RES MF 680K 1/4W 2%	24773-342K
R3	RES MF 10K 1/4W 2%	24773-297M
R4	RES MF 10K 1/4W 2%	24773-297M
R5	RES MG 10M 1/4W 5%	24321-885W

Circuit reference	Description	Mfr./Part Number
Unit AF02 - Keyboard decoder - (continued)		
R6	RES MF 100K 1/4W 2%	24773-321L
R7	RES MF 10K 1/4W 2%	24773-297M
R8	RES MF 15K 1/4W 2%	24773-301P
R9	RES MF 100K 1/4W 2%	24773-321L
R10	RES MF 270K 1/4W 2%	24773-331D
R11	RES MF 270K 1/4W 2%	24773-331D
R12	RES MF 10K 11/4W 2%	24773-297M
R13	RES MF 15K 1/4W 2%	24773-301P
R14	RES MF 56K 1/4W 2%	24773-315U
R15	RES MF 100K 1/4W 2%	24773-321L
R16	RES MF 100K 1/4W 2%	24773-321L
R17	RES MF 100K 1/4W 2%	24773-321L
R18	RES MF 100K 1/4W 2%	24773-321L
R19	RES MF 100K 1/4W 2%	24773-321L
R20	RES MF 100K 1/4W 2%	24773-321L
R21	RES MF 100R 1/4W 2%	24773-249J
R22	RES MF 100R 1/4W 2%	24773-249J
R23	RES MF 10K 1/4W 2%	24773-297M
R24	RES MF 10K 1/4W 2%	24773-297M
R25	RES MF 2K2 1/4W 2%	24773-281Y
R26	RES MF 10K 1/4W 2%	24773-297M
R27	RV CERM 10K LIN .3W 10% FLAT	25748-507X
SK1	CON PCB G08D20A9 BM BA-C	ITT CANNON SINGLE SOURCE
SK2	CON MIN 143-105	MOLEX 22-04-1031 SINGLE SOURCE
TR1	TR NSI 2N2369 15V 500M-SW	28452-197H
TR2	TR NSI 2N2369 15V 500M-SW	28452-197H
TR3	TR NSI 2N2369 15V 500M-SW	28452-197H
TR4	TR NJF 2N4339 50V	28459-023B

Circuit reference	Description	Mfr./Port Number

Unit AF03/1 - Signal input board -

18. When ordering, prefix circuit reference with AF03/1

	Complete unit	3964-129
C1	CAP CER .01UF 25V 20%	26383-006C
C2	CAP TANT .047UF 35V 20%	26486-207L
C3	CAP TANT 4.7UF 35V 20%	26486-219P
C4	CAP TANT 4.7UF 35V 20%	26486-219P
C5	CAP TANT 4.7UF 35V 20%	26486-219P
C6	CAP TANT 10UF 35V 20%	26486-225C
C7	CAP TANT 10UF 35V 20%	26486-225C
C8	CAP TANT 1.0UF 35V 20%	26486-209F
C10	CAP CER .01UF 50V 20%	26383-534Y
C11	CAP CER .001UF 63V 10%	26383-585M
C12	CAP CER .01UF 25V 20%	26383-006C
C13	CAP CER .01UF 25V 20%	26383-006C
C14	CAP CER 4P7 63V .25PF	26343-461B
C101	CAP PETP .01UF 400V 10%	26582-232W
C102	CAP CER 100PF 63V 2%	26343-477U
C103	CAP TANT 10UF 35V 20%	26486-225C
C104	CAP TANT .047UF 35V 20%	26486-207L
C105	CAP TANT 1.0UF 35V 20%	26486-209F
C106	CAP TANT 1.0UF 35V 20%	26486-209F
C109	CAP CER 100PF 63V 2%	26343-477U
C110	CAP CER 100PF 63V 2%	26343-477U
C111	CAP CER 56PF 63V 2%	26343-474J
C112	CAP TANT 1.0UF 35V 20%	26486-209F
C113	CAP TANT 1.0UF 35V 20%	26486-209F
C201-C213, and C301-C313	are identical values to the series C101-C113 listed above.	
D1	DIODE ZEN 1N825/A 6.2V 5%	28371-494Z
D2	DIODE ZEN BZX79 12V 5%	28372-149G
D3	DIODE RECT 1N4004	28357-028K
D4	DIODE RECT 1N4004	28357-028K
D103	DIODE SIL 1N4148	28336-676J
D104	DIODE SIL 1N4148	28336-676J
D203,D204 and D303,D304	are identical values to D103, D104.	

Circuit reference	Description	Mfr./Part Number
Unit AF03/1 - Signal input board - (continued)		
IC1	ICA MUX DG 508BP 8 INP !	28469-361C
IC2	ICA AMP OP27GZ	28461-368T
IC3	ICD AND 4081 QUAD 2 INP BI !	28466-009L
IC4	ICD NAND 4011 QUAD 2 INP B! !	28466-340R
IC5	ICA MUX CD 4052B DUAL !	RCA
IC6	ICA AMP TL 071CP FET 1/P DIL 8	28461-347A
IC7	ICA VREG MC 78L05CP	MOTOROLA
IC101	ICA AMP OP27GZ	28461-368T
IC201,IC202 and IC301,IC302	are identical types to IC101,IC102	
PL1	90^0 SQ PIN (WITH LOCK)	TOOL NO. 7966
R1	RES MF 10K 1/4W 2%	24773-297M
R2	RES MF 10K 1/4W 2%	24773-297M
R3	RES MF 10K 1/4W 2%	24773-297M
R4	RES MF 3K3 1/4W 2%	24773-285F
*R5	RES MF 422K 1/4W 0.5%	TO SPEC 24700-003
R6	RV CERM 10K	25748-566S
R7	RES MF 1/4W 0.5%	24753-624H
R8	RES MF 1/4W 0.5%	24753-621K
R9	RES MF 1/4W 0.5%	TO SPEC 24700-003
R10	RES MF 7K87 1/4W 0.5%	24753-591U
R11	RES MF 150R 1/4W 2%	24773-253F
R13	RES MF 100K 1/4W 2%	24773-321L
R14	RES MF 100K 1/4W 2%	24773-321L
R15	RES MF 1K 1/4W 2%	24773-273A
R16	RES MF 10K 1/4W 2%	24773-297M
R17	RES MF 27K 1/4W 2%	24773-307K
R18	RES MF 10K 1/4W 2%	24773-297M
R19	RES MF 10R 1/4W 2%	24773-225W
R101	RES MF 39K 1/4W 2%	24773-311A
R102	RES MF 15R 1/4W 2%	24773-229X
R103	RES MF 15R 1/4W 2%	24773-229X
*R104	RES MF 150K 1/4W 2%	24773-325V
R105	RV 20K LIN 1/2W 10%	25748-565V
R106	RES MF 330R 1/4W 2%	24773-261D
R107	RES MF 39R 1/4W 2%	24773-239Z

Circuit reference	Description	Mfr./Part Number
Unit AF03/1 - Signal input board - (continued)		
R108	RES MF 2K2 1/4W 2%	24773-281Y
R109	RES MF 10K 1/4W 2%	24773-297M
R110	RES MF 39K 1/4W 2%	24773-311A
R112	RES MF 47K 1/4W 2%	24773-313H
R115	RES MF 47K 1/4W 2%	24773-313H
R116	RES MF 10K 1/4W 2%	24773-297M
R117	RES MF 2K7 1/4W 2%	24773-283L
R118	RES MF 1K 1/4W 2%	24773-273A
R119	RV 2K 1/2W 10%	25748-562J
R124	RES MF 1K 1/4W 2%	24773-273A
R125	RES MF 1K 1/4W 2%	24773-273A
R126	RES MF 100K 1/4W 2%	24773-321L
R127	RES MF 82K 1/4W 2%	24773-319V
R128	RES MF 8K2 1/4W 2%	24773-295P
R201-R228 and R301-R328	are identical values to R101-R128.	
SK1	CON RF SMB MALE 50Ω PCB ELBOW	23444-359Z
	SOCKET PW SPRING	28488-009N
SK	LOW PROFILE DIL 16	28488-041E
TR1	TR NSI 2N2369 15V 500M-SW	28452-197H
TR101	TR NJF J310 !	28459-028E
TR102	TR NJF J310 !	28459-028E
TR103	TR NSI BC414	MOTOROLA
TR201-TR203 and TR301-TR303	are identical types to TR101-TR103.	

Unit AF04 - Intensity control -

19. When ordering, prefix circuit reference with AF04

	Complete unit	3964-021
R1	RES MF 75R 1/4W 2%	24773-246Y
R2	RES MF 470R 1/4W 2%	24773-265M
R3	RES MF 1K5 1/4W 2%	24773-277U
R4	RES MF 1K5 1/4W 2%	24773-277U
R5	RES MF 1K5 1/4W 2%	24773-277U

Circuit reference	Description	Mfr./Part Number
Unit AF04 - Intensity control - (continued)		
R6	RV 1K	BOURNS 82C1A-E28-A10
R7	RV 1K	BOURNS 82C1A-E28-A10
R8	RV 1K	BOURNS 82C1A-E28-A10
R9	RV 1K	BOURNS 82C1A-E28-A10

Unit AM01 - Part of General assembly -

20. When ordering, prefix circuit reference with AM01

Circuit reference	Description	Mfr./Part Number
	Complete unit	3964-080
SK1-SK12	EDGE CONNECTOR MKD-32D-P-01-01	PYE CONNECTORS
SK13	CONN PCB	ITT CANNON
SK14	CONN PCB	ITT CANNON
SK15	CONN 2.5MM PITCH 5046-A90%(10 SQ PINS)	MOLEX 22-05-1102
SK17	CONN 2.5MM PITCH 5046-A90%(8 SQ PINS)	MOLEX 22-05-1082

Unit AR01 - ±15V Regulator -

21. When ordering, prefix circuit reference with AR01

Circuit reference	Description	Mfr./Part Number
	Complete board	3964-097
C1	CAP ELEC 470UF 63V 20% AX	26415-842Z
C2	CAP CER .01UF 25V 20% DISC	26383-006C
C3	CAP TANT 4.7UF 35V 20% BEAD	26486-219P
C4	CAP ELEC 470UF 63V 20% AX	26415-842Z
C5	CAP CER .01UF 25V 20% DISC	26383-006C
C6	CAP TANT 4.7UF 35V 20% BEAD	26486-219P
D1	DIODE BRIDGE 2KBB20R 200V 1.9A	28359-189D
D2	DIODE RECT 1N4004 400V	28357-028K
D3	DIODE RECT 1N4004 400V	28357-028K
D4	DIODE BRIDGE 2KBB20R 200V	28359-189D
D5	DIODE RECT 1N4004 400V	28357-028K
D6	DIODE RECT 1N4004 400V	28357-028K
IC1	ICA VREG+ 7815 15V 1A TO220	28461-709S
IC2	ICA VREG- 7915 15V 1A TO220	28461-735N

Circuit reference	Description	Mfr./Part Number

Unit AR02 - ±15V Regulator -

22. When ordering, prefix circuit reference with AR02

	Complete board	3964-077
C1	CAP ELEC 470UF 63V 20% AX	26415-842Z
C2	CAP CER .01UF 25V 20% DISC	26383-006C
C3	CAP TANT 4.7UF 35V 20% BEAD	26486-219P
C4	CAP ELEC 470UF 63V 20% AX	26415-842Z
C5	CAP CER .01UF 25V 20% DISC	26383-006C
C6	CAP TANT 4.7UF 35V 2% BEAD	26486-219P
D1	DIODE BRIDGE 2KBB20R 200V 1.9A	28359-189D
D2	DIODE RECT 1N4004 400V	28357-028K
D3	DIODE RECT 1N4004 400V	28357-028K
D4	DIODE BRIDGE 2KBB20R 200V	28359-189D
D5	DIODE RECT 1N4004 400V	28357-028K
D6	DIODE RECT 1N4004 400V	28357-028K
D7	DIODE RECT 1N4004 400V	28357-028K
D8	DIODE RECT 1N4004 400V	28357-028K
IC1	ICA VREG+ 7815 15V 1A TO220	28461-709S
IC2	ICA VREG- 7915 15V 1A TO220	28461-735N

Unit AR03 - +12V Regulator -

23. When ordering, prefix circuit reference with AR03

	Complete board	3964-098
C1	CAP TANT 10UF 35V 20%	26486-225C
C2	CAP TANT 4.7UF 35V 20%	26486-219P
C3	CAP TANT 4.7UF 35V 20%	26486-219P
D1	DIODE RECT 1N4004 400V	28357-028K
D2	DIODE RECT 1N4004 400V	28357-028K
IC2	ICA(MOUNTED ON H.S.1)VREG+LM 317K PROG 1A5 T)3	28461-728H
R1	1K8 1/4W 2%	24773-279N
R2	220R 1/4W 2%	24773-257W

Circuit reference	Description	Mfr./Part Number

Unit AR04/1 - Ramp circuit -

24. When ordering, prefix circuit reference with AR04/1

	Complete board	3964-126
C1	CAP TANT 10UF 35V 20% BEAD	26486-225C
C2	CAP TANT 1.0UF 35V 20% BEAD	26486-209F
C3	CAP TANT 10UF 35V 20% BEAD	26486-225C
C4	CAP PETP .1UF 100V 10% RAD	26582-211B
C5	CAP PETP .1UF 100V 10% RAD	26582-211B
IC1	ICA AMP TL072CP DUAL FET 1/P	28461-348Z
IC2	ICA 79L12	MOTOROLA MC79L12 CP-12V-0A OR NAT.S LM340 LAZ-12
IC3	ICA AMP TL072CP DUAL FET 1/P	28461-348Z
L1	INDUCTOR (SPECIAL) 65 μH PARALLEL WITH 1K	3964/328
L2	INDUCTOR (SPECIAL) 65 μH PARALLEL WITH 1K	3964/328
PL1	CON 3-WAY FRICTION LOCK	23435-870Y
R1	RES MF 10K 1/4W 2%	24773-297M
R2	RES MF 3K3 1/4W 2%	24773-285F
R3	RES MF 3K9 1/4W 2%	24773-287V
R4	RV CERM 1K LIN 10%	BOURNS 3299W-1-102 OR SPECTROL 52W/1K
R5	RV CERM 5K LIN 10%	BOURNS 3299W-1-502 OR SPECTROL 52W/5K
R6	RV CERM 5K LIN 10%	BOURNS 3299W-1-502 OR SPECTROL 52W/5K
R7	RES MF 18K 1/4W 2%	24773-303M
R8	RES MF 220K 1/4W 2%	24773-329T
R9	RES MF 20K 1/4W 2%	24773-304C
R10	RES MF 100K 1/4W 2%	24773-321L
R11	RES MF 560R 1/4W 2%	24773-267R
R12	RES MF 1K5 1/4W 2%	24773-277U
R13	RES MF 100R 1/4W 2%	24773-249J
R14	RES MF 100R 1/4W 2%	24773-249J
SK1	CON RF SMB 50 PCB ST	23444-334Y
SK2	CON RF SMB 50 PCB ST	23444-334Y

Circuit reference	Description	Mfr./Part Number

Unit AR05 - +24V Regulator -

25. When ordering, prefix circuit reference with AR05

	Complete board	3964-100
C1	CAP ELEC 470UF 63V 20% AX	26415-842Z
C2	CAP TANT 10UF 35V 20% BEAD	26486-225C
C3	CAP PETR .1UF 100V 10% RAD	26582-211B
C4	CAP TANT 10UF 35V 20% BEAD	26486-225C
D1	DIODE BRIDGE 2KBB20R 200V 1.9A	28359-189D
D2	DIODE ZEN BZX 79C30	MOTOROLA OR MULLARD
D3	DIODE RECT 1N4004 400V	28357-028K
D4	DIODE RECT 1N4004 400V	28357-028K
IC1	ICA VREG MC 78L24ACP	MOTOROLA
R1	RES MF 1K2 1/4W 2%	24773-275H
TR1	TR TIP 120	FAIRCHILD OR TEXAS

Unit AR06 - Power supply chassis assy. -

26. When ordering, prefix circuit reference with AR06

C7	CAP ELEC 10000UF 40V 10% TAGS	26426-096B
C8	CAP ELEC 10000UF 25V 10% TAGS	26426-095R
C9	CAP ELEC 10000UF 25V TAGS	26426-095R
C10	CAP ELEC 10000UF 25V 10% TAGS	26426-095R
FS1	FUSE TIME LAG 600mA	FARNELL
FS2	FUSE TIME LAG 600mA	FOR 240V APPLICATION PT No. TDC 123 600mA.
FS1	FUSE TIME LAG 1.25A	FARNELL
FS2	FUSE TIME LAG 1.25A	FOR 115V APPLICATION PT No. TDC 123 1.25A
	FUSE HOLDER (FOR FS1 & FS2) 20X50 mm	23416-192R
SK1	CONNECTOR/MAINS FILTER MALE 3 FXD RF FILTER	23423-150L
S1	SW PB SWITCH MSAM TYPE	ITT SWITCHES (U.K.) LTD.
S2	SW SLIDE 2CO PANEL MTG	23467-161W
T1	TXFRM MAINS	3964-149

Circuit reference	Description	Mfr./Part Number

Unit AR07 - Part of Power supply chassis -

27. When ordering, prefix circuit reference with AR07

FS3-FS7	FUSE LINK 250mA T-D	RADIO RESISTORS
	FUSE HOLDER (FOR FS3-FS7)	RADIO RESISTORS
R1	RES MO 330R 1/2W 2%	24573-061U

Unit AR09 - Heat sink assy 1 -

28. When ordering, prefix circuit reference with AR09

D2	DIODE BRIDGE BY260 200V	28359-190S
IC2	ICA VREG LM317K PROG 1A5 TO3	28461-728H

Unit AR10 - Heat sink assy. 2 -

29. When ordering, prefix circuit reference with AR10

C2	CAP TANT 10UF 35V 20%	26486-225C
C3	CAP TANT 4.7UF 35V 20%	26486-219P
D1	DIODE BRIDGE BY260	28359-190S
D2	DIODE RECT 1N4004 400V	28357-028K
IC1	ICA VREG UA78H05SC	FAIRCHILD
	OR ICA VREG LAS1905	LAMBDA

Unit AT01/1 - Part of CRT -

30. When ordering, prefix circuit reference with AT01/1

	Complete board	3964-137
C1	CAP ELECT 1000UF 35V 20%	26421-130W
C2	CAP CER .1UF 50V 20%	26383-534Y
C3	CAP ELEC 100UF 35V 20%	26421-122J
C4	CAP PETP .1UF 63V 10%	26582-429F
C5	CAP PETP .1UF 63V 10%	26582-429F
C6	CAP PETP .1UF 63V 10%	26582-429F

Circuit reference	Description	Mfr./Part Number
Unit AT01/1 - Part of CRT - (continued)		
C7	CAP CER 33P 63V 5%	26343-471Y
C8	CAP ELEC 4UF 35V 20%	26421-108A
C9	CAP CER .1UF 50V 20%	26383-534Y
C10	CAP ELEC 2200U 16V 20%	26421-132T
C11	CAP CER 1000P 63V 10%	26383-585M
C12	CAP ELEC 100UF 35V 20%	26421-122J
C13	CAP PETP .1UF 63V 10%	26582-429F
C14	CAP CER 470P 63V 10%	26383-582T
C15	CAP CER 470P 63V 10%	26383-582T
C16	CAP PETP .1UF 63V 10%	26582-429F
C17	CAP PETP .01UF 63V 10%	26582-426N
C18	CAP CER 1000P 63V 10%	26383-585M
C19	CAP CER 1000P 63V 10%	26383-585M
C20	CAP ELEC 4U7 35V 20%	26421-102A
C21	CAP PETP .01UF 63V 10%	26582-426N
C22	CAP CER 1000P 63V 10%	26383-585M
C23	CAP PETP .47UF 63V 10%	26582-427L
C24	CAP PP .012UF 630V 10%	26582-490E
C25	CAP ELEC 100UF 35V 20%	26421-122J
C26	CAP ELEC 33UF 250V -10+50%	26421-134X
C27	CAP ELEC 1UF 63V 20%	26423-201V
C28	CAP PETP .1UF 630V 10%	26582-228S
C29	CAP PETP .002UF 250V 10%	26582-204X
C30	CAP PETP 3.3UF 100V 10%	26582-229W
C31	CAP PETP .1UF 250V 10%	26582-208B
D1	DIODE RECT 1N4004 400V	28357-028K
D2	DIODE SIL 1N4148 75V	28336-676J
D3	DIODE SIL 1N4148 75V	28336-676J
D4	DIODE SIL 1N4148 75V	28336-676J
D5	Diode RECT MR854 400V	28357-016W
D6	DIODE RECT BYW95C 600V	28358-726P
D7	DIODE RECT BA159 1000V	28359-103B
D8	DIODE RECT BYW95C 600V	28358-726P
D9	DIODE RECT BA159 1000V	28359-103B
D10	DIODE RECT BY584 1800V	28359-105A
IC1	VERT DEFLECTION SYSTEM TDA 1170S	28231-408A
IC2	ICD MONO 555 TIMER	23468-304P
IC3	ICD MONO 555 TIMER	28468-304P

Circuit reference	Description	Mfr./Part Number
Unit AT01/1 - Part of CRT - (continued)		
L1	IND (WIDTH CONTROL)	SAREA
L2	IND (LIN.CONTROL)	28231-401P
PL1	CON PCB MALE 8-WAY	23435-872L
PL2	CON PART M/W FEM 4-WAY	MOLEX 03-09-1041
R1	RES MF 220K 1/4W 2%	24773-329T
R2	RES MF 150K 1/4W 2%	24773-325Y
R3	RV CERM 100K LIN 1/2W 10%	25711-644W
R4	RES MF 390K 1/4W 2%	24773-335M
R5	RES MF 39K 1/4W 2%	24773-311A
R6	RV CERM 100K LIN 1/2W 10%	25711-644W
R7	MF 470K 1/4W 2%	24773-337R
R8	RES MF 220K 1/4W 2%	24773-329T
R9	RES MF 56K 1/4W 2%	24773-315U
R10	RES MF 68K 1/4W 2%	24773-317M
R11	RES MF 1R 1/4W 2%	24773-201M
R12	RES MF 56K 1/4W 2%	24773-315U
R13	RES MF 3R3 1/4W 2%	24773-213U
R14	RES MF 100K 1/4W 2%	24773-321L
R15	RES MF 68R 1/4W 2%	24773-245U
R16	RES MF 390R 1/4W 2%	24773-263P
R17	RV CERM 1K LIN 1/2W 10%	25711-638G
R18	RES MF 470R 1/4W 2%	24773-265M
R19	RES MF 1K 1/4W 2%	24773-273A
R20	RES MF 150R 1/4W 2%	24773-253F
R21	RES WW 3K3 3W 5%	25125-094W
R23	RES MO 18R 1/2W 2%	24573-031N
R24	RES MF 6K8 1/4W 2%	24773-293D
R25	RES MF 10K 1/4W 2%	24773-297M
R26	RES MF 5K6 1/4W 2%	24773-291S
R27	RES MF 5K6 1/4W 2%	24773-291S
T1	TR XFR (EHT) SUP TBT6	28231-402X
TR1	TR PSI BC308B 20V	28433-455R
TR2	TR NSI BF338 225V	28458-577X
TR3	TR NSI BC209C 20V	28452-771P
TR4	TR NSI BC209C 20V	28452-771P
TR5	TR PSI BC308B 20V	28433-455R
TR6	TR NSI BU806 400V	28458-690K
TR7	TR NSI BF338 225V	28458-577X OR ERIE TYPE 00026/012

Circuit reference	Description	Mfr./Part Number

Unit AT02 - Part of CRT -

31. When ordering, prefix circuit reference with AT02

	Complete board	3964-066
C17	CAP CER 33pF 100V 20%	MULLARD 632 SERIES PART NO. 63234339
R4	RES 330R 1/2W 10%	ALLEN BRADLEY TYPE EB OR ERIE TYPE 00026/012
R5	RES 22K 1/2W 10%	ALLEN BRADLEY TYPE EB OR ERIE TYPE 00026/012
R6	RES 22K 1/2W 10%	ALLEN BRADLEY TYPE EB OR ERIE TYPE 00026/012
R7	RES 1K5 1/2W 10%	ALLEN BRADLEY TYPE EB

Unit GPIB - Interface module - (Optional accessory)

32. When ordering, prefix circuit reference with GPIB interface

	Complete GPIB module (Option 001)	3964-650
	PCB assy.	3964-301
	Switch, p.c.b. assy.	3964-302
	Cable assy.	3964-601
C1	CAP CER .01UF 25V 20%	26383-006C
C2	CAP CER .01UF 25V 20%	26383-006C
C3	CAP CER .01UF 25V 20%	26383-006C
C4	CAP CER .01UF 25V 20%	26383-006C
C5	CAP CER .01UF 25V 20%	26383-006C
C6	CAP CER .01UF 25V 20%	26383-006C
C7	CAP CER .01UF 25V 20%	26383-006C
C8	CAP TANT 47UF 6V 20%	26486-232A
CABLE	24-WAY RIBBON FLAT	15360-893A
CON	20-WAY PLUG SOLDER/TRANS	23435-860B
		ITT CANNON GO & D
CON	20-WAY SOCKET IDC	029-8504-000
IC1	ICD MP SUP 8291A GPIB TALK/LIS !	28467-014C
IC2	ICD BUFF 3448 QUAD GPIB TXTX 3S	28469-190R
IC3	ICD BUFF 3448 QUAD GPIB TXTX 3S	28469-190R
IC4	ICD BUFF 3448 QUAD GPIB TXTX 3S	28469-190R
IC5	ICD BUFF 3448 QUAD GPIB TXTX 3S	28469-190R
IC6	ICD NAND 74LS00 QUAD 2 1NP	28466-345H
IC7	74LS367	TEXAS SNN74LS367AN OR NAT.S DM74LS367N
R1-R6	RES NET 4K7 1/4W 2%	24681-608D

Circuit reference	Description	Mfr./Part Number
Unit GPIB - Interface module - (Optional accessory) (continued)		
R7	RES MF 4K7 1/4W 2%	24773-289W
R8	RES MF 4K7 1/4W 2%	24773-289W
SW	6-WAY DIL	23465-897W

MECHANICAL COMPONENTS

33. Order without prefix

Fig. 1 Item	Description	Mfr./Part Number
1	Front panel keyboard detail	3964-188
2	Front panel c.r.t. bracket assy.	3964-152
3	CRT tinted filter	3964-191
4	Front trim (upper)	3964-197
	Front trim (lower)	3964-198
5	Front trim infill	3964-199
6	Side panel assy.	3964-158
7	Clamp card retainer assy.	3964-009
8	Rear panel assy.	3964-174
9	Rear trim	3964-200
10	Top cover	3964-150
11	Voltage selector plate	3964-156
12	End cap (two parts)	3964-103
	End cap (two parts)	3964-104
13	Side trim infill	3964-159
14	Side rail	3964-158
15	Side handle cover moulding	3964-102
16	Handle bush	3964-111
17	Handle cover	3964-100
	Handle spring (2 off)	3964-099
18	Bottom cover (complete with tilt stand and feet)	3964-178
19	Rear foot	37590-224R
20	Rear foot stud	37590-223C
21	Front foot	37590-253X
	Tilt stand	37590-254M
22	Screw c'sk posidrive chrome (M4 x 16 LG) MS	
23	Screw cup washer	21171-550W
24	Front handle infill	3964-203
25	Front handle	3964-241
26	Handle moulding	3964-106
27	Knob assy. 20 mm	41149-061W
	Knob assy cap (stone grey)	37590-281W
28	Intensity control (AF04) assy.	3964-023
29	AM01 card frame assy.	3964-011
	Card guide	3964-246
	Front card bracket assy.	3964-164
	Rear card bracket assy.	3964-165
	Card frame bracket assy.	3964-172
30	Knob assy. 10.5 dia. x 4 mm (dark brown)	41149-037B
	Knob assy. cap (stone grey)	37590-242F

Chapter 7

SERVICING DIAGRAMS

CONTENTS

CIRCUIT NOTES

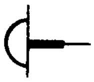
Component values

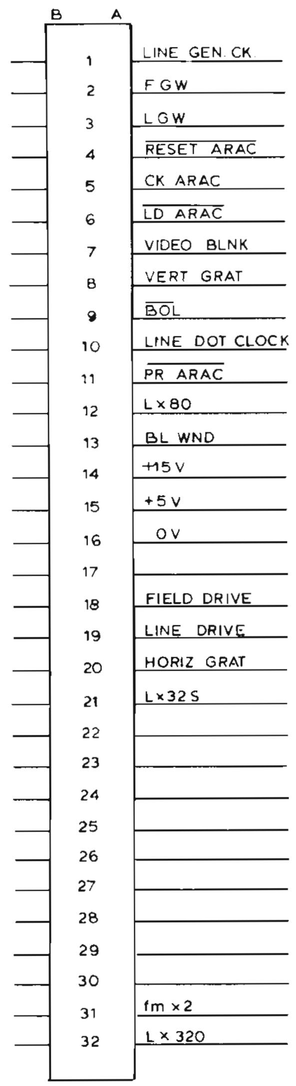
1. Resistors : Code letter R=ohms, k=kilohms (10^3), M=megohms (10^6).
   Capacitors : Code letter m=millifarads (10^{-3}), μ=microfarads (10^{-6}), n=nanofarads (10^{-9}), p=picofarads (10^{-12}).
   Inductors : Code letter H=henrys, m=millihenrys (10^{-3}), μ=microhenrys (10^{-6}), n=nanohenrys (10^{-9}).
   SIC : Value selected during test, nominal value shown.

2. Components are marked normally with two, three or four figures according to the accuracy limit ±10%, ±1% or ±0.1%. The code letter used indicates the multiplier and replaces the decimal point. Because a marking 4m7 could be interpreted as milliohms, millifarads or millihenrys, all values are placed near to its related symbol.

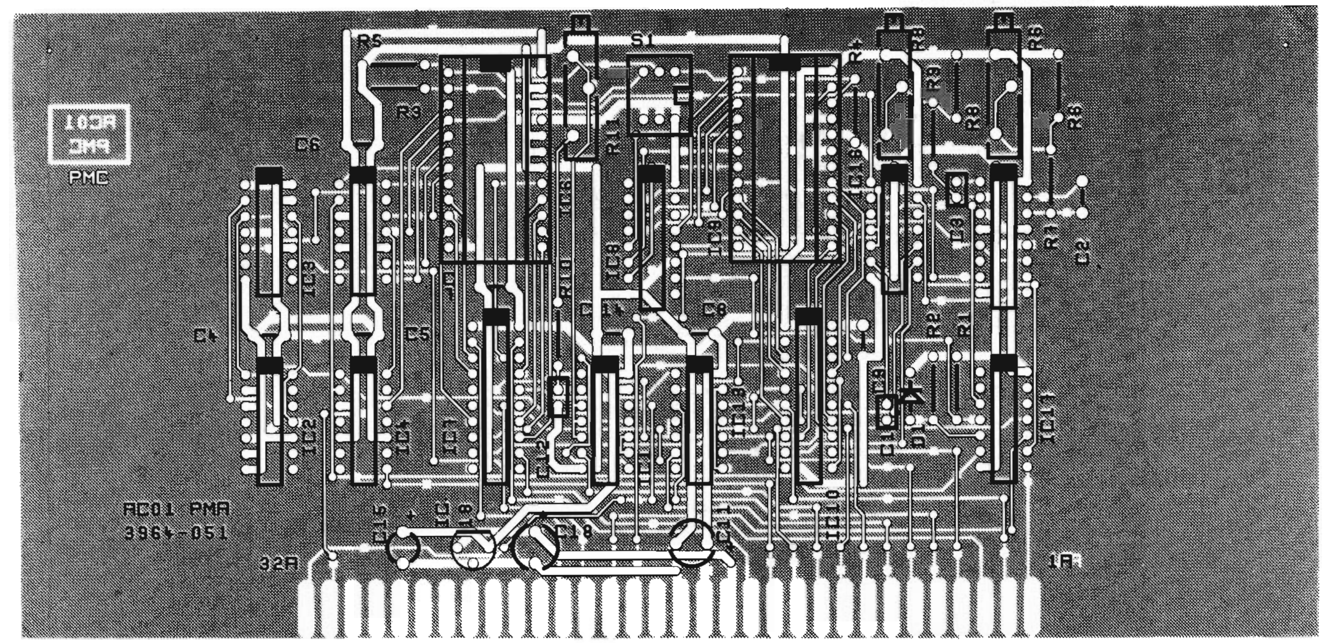
Symbols

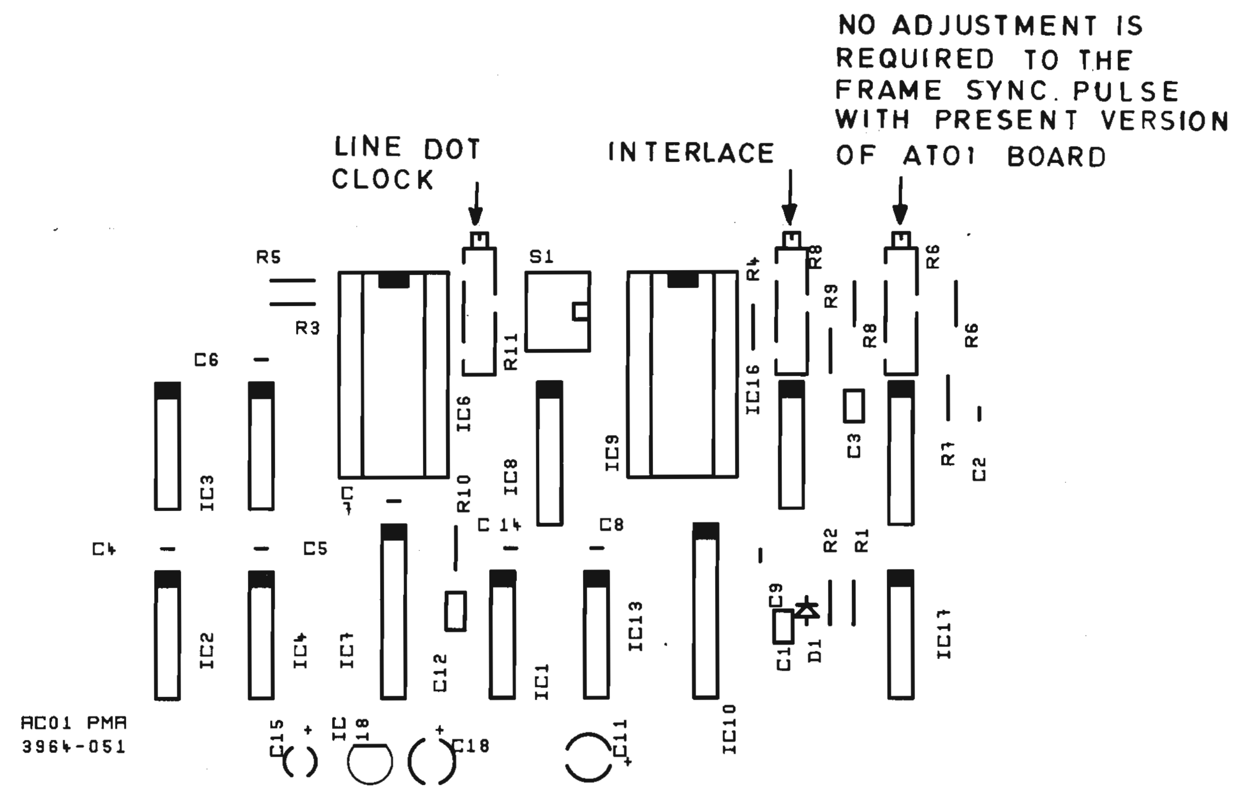
3. Symbols are based on the provisions of BS 3939 with the following additions :

A14		Edge connector (board contact A14)
	⚠	Warning, see Notes and Cautions
TP1		Test point



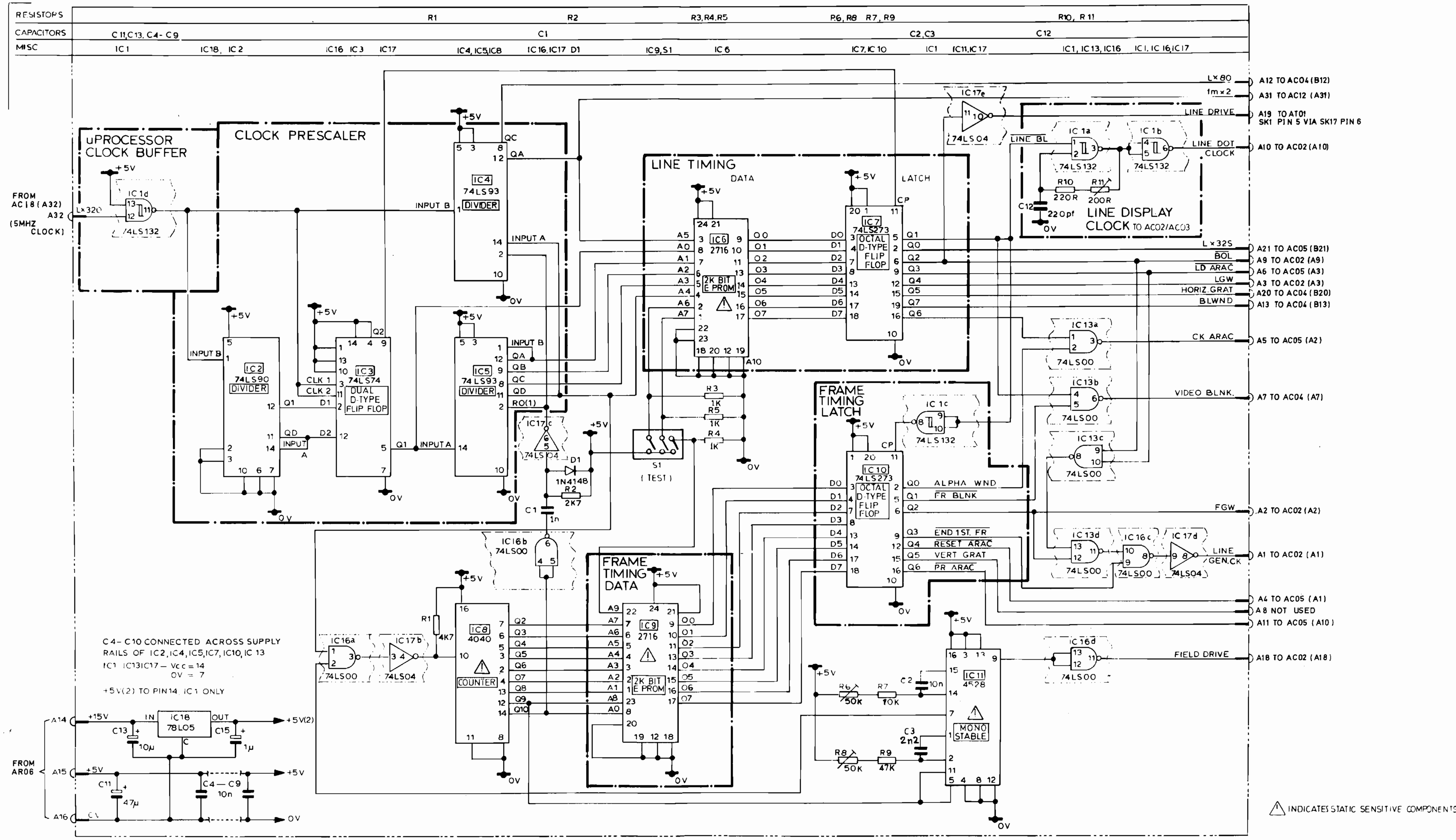
EDGE CONNECTOR VIEWED FROM UNDERSIDE OF MOTHER BOARD.





ACO1

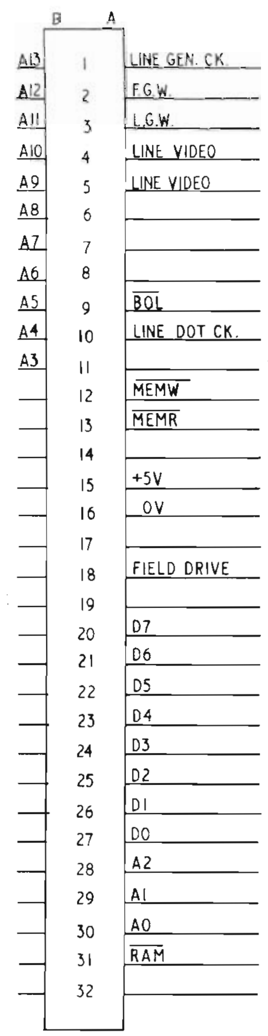
Fig. 1a Component layout and edge connector connections, AC01



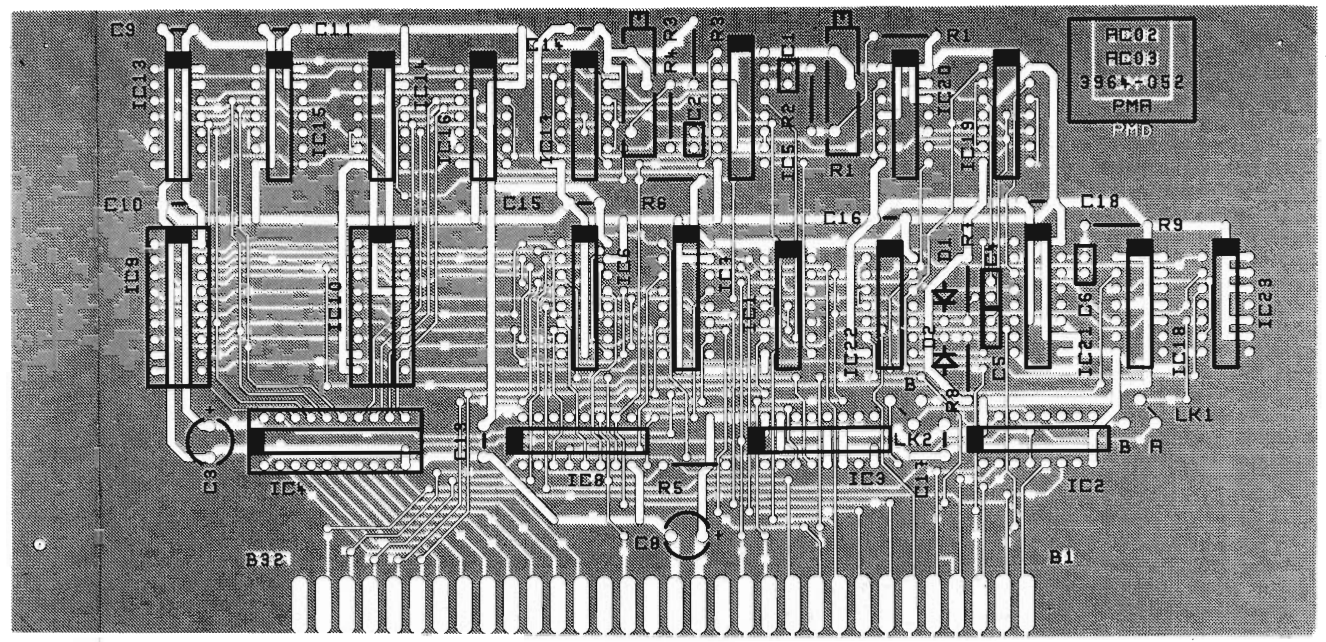
ACO1

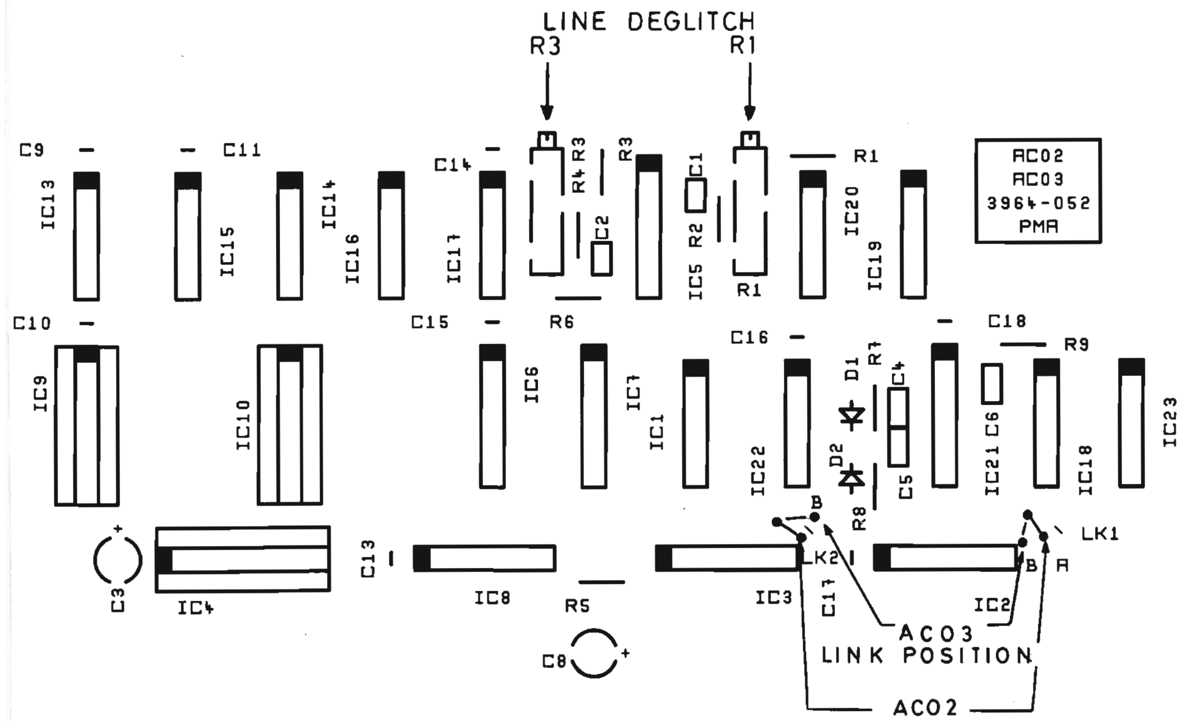
3964/901, Iss. 2

Fig. 1 Timing circuit, ACO1



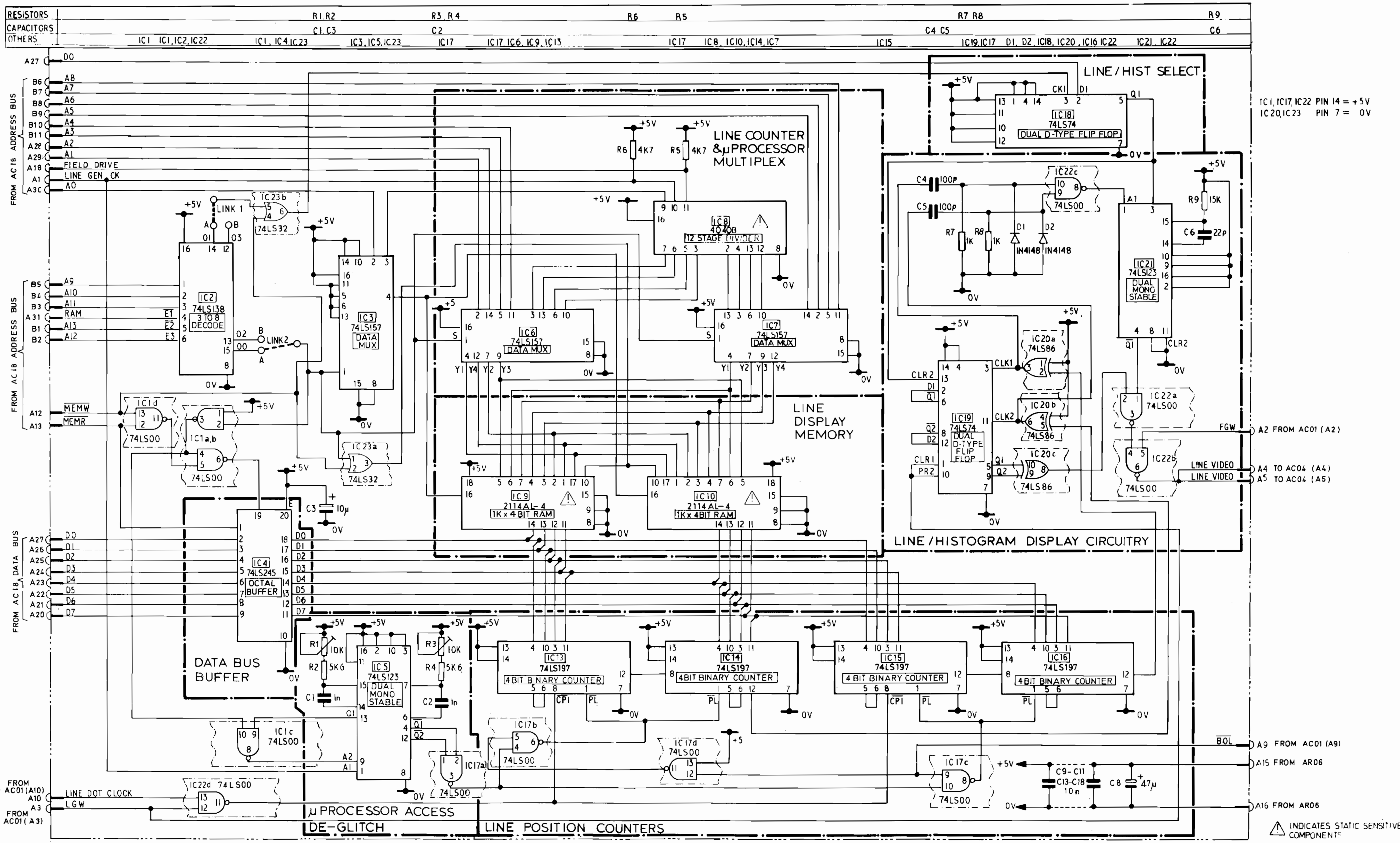
EDGE CONNECTOR VIEWED FROM UNDERSIDE OF MOTHER BOARD





AC02/3

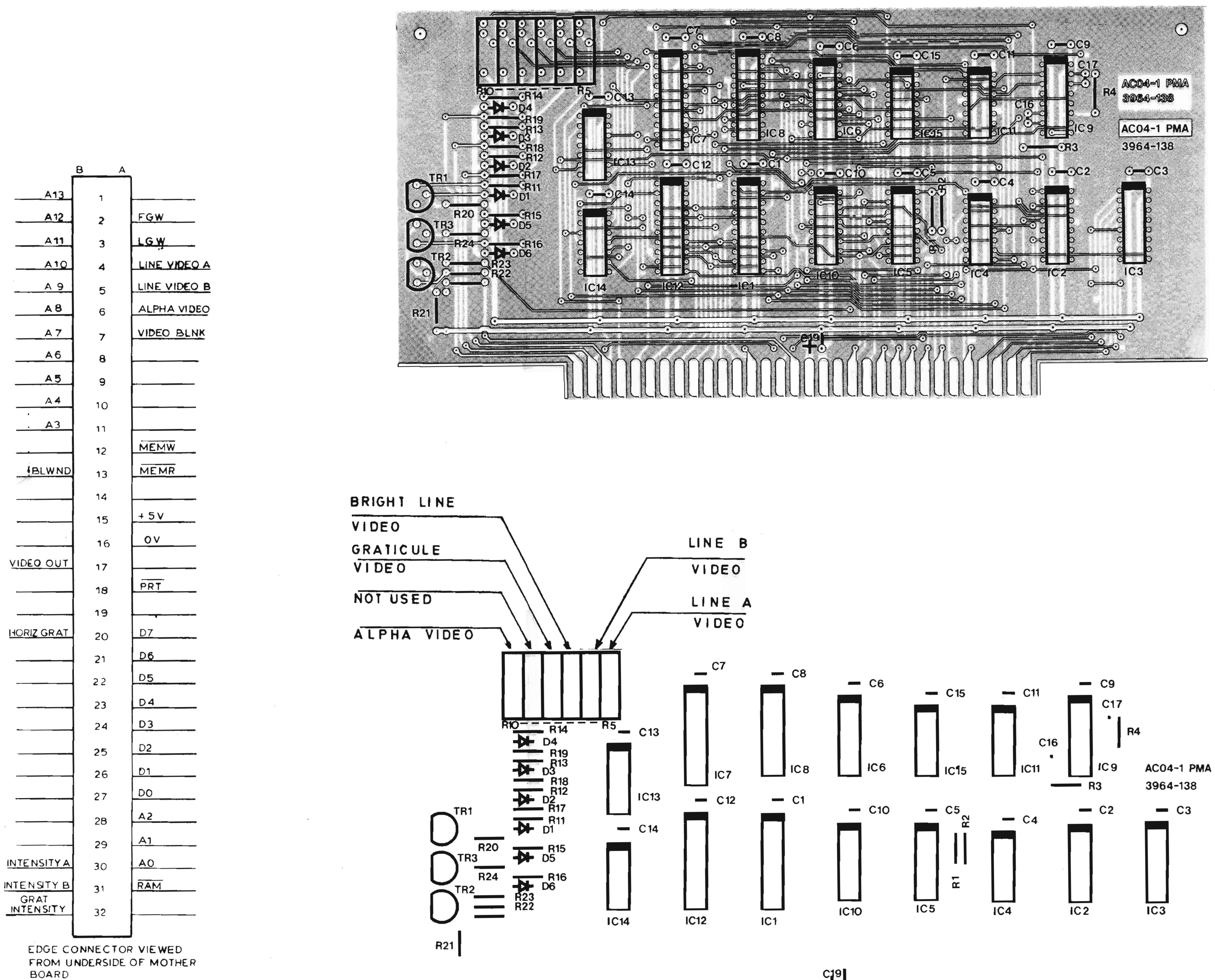
Fig. 2a Component layout and edge connector connections, AC02/AC03



3964/902, Iss. 1
3964/903, Iss. 1

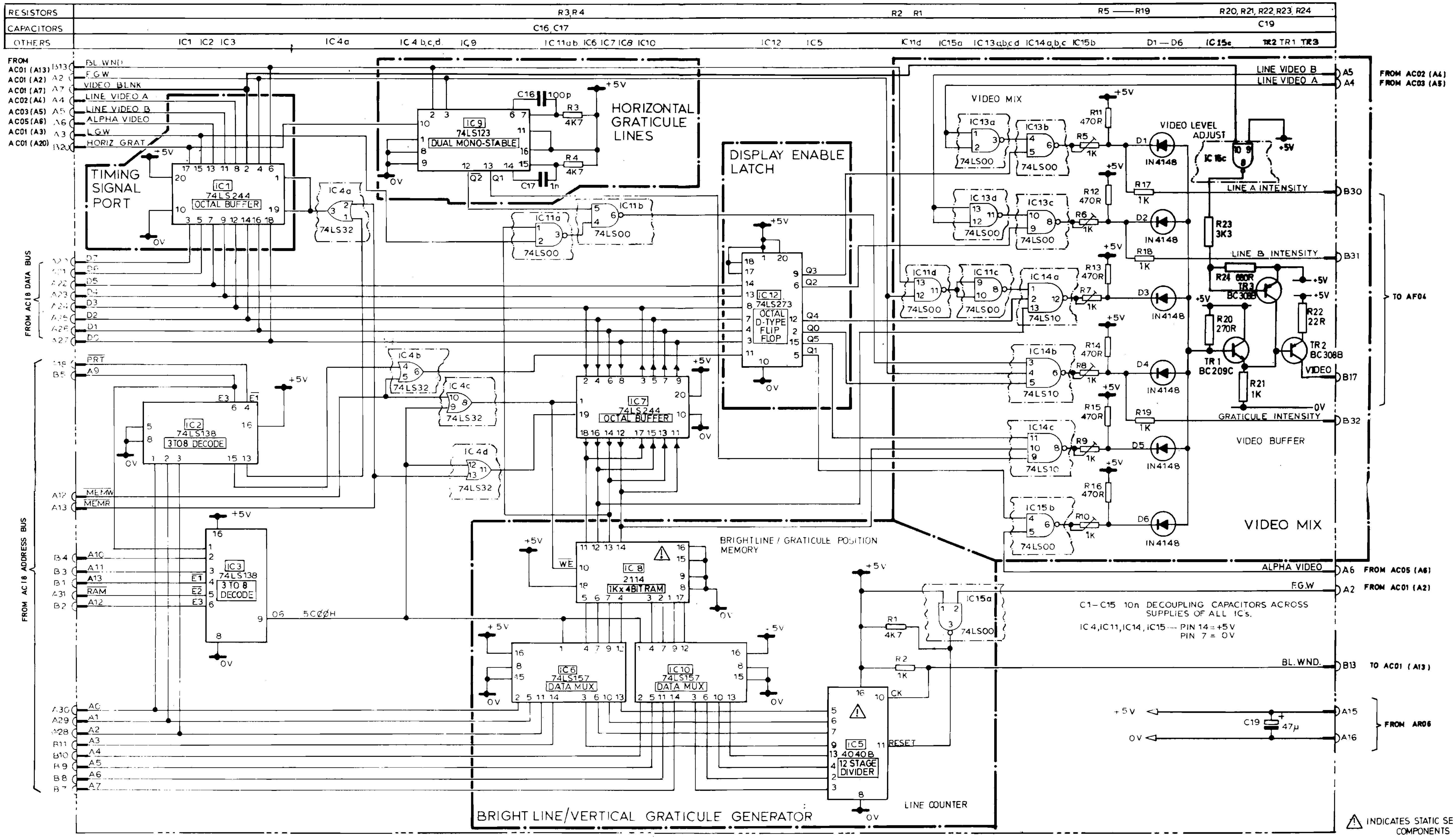
ACO2/3

Fig. 2 Line generators A and B, AC02/AC03



AC04/1

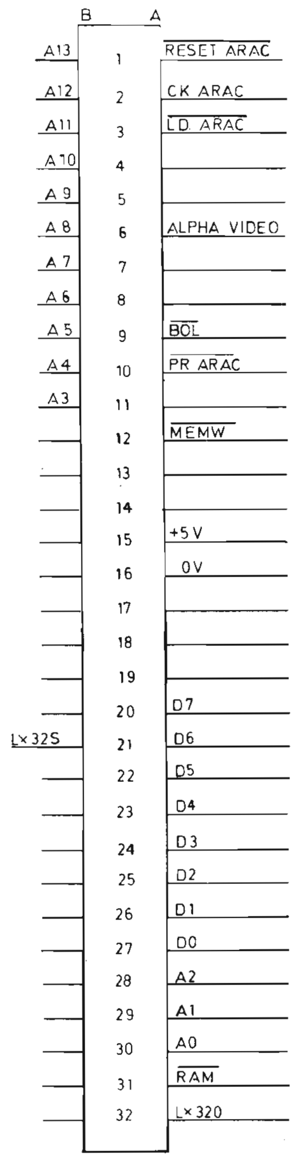
Fig. 3a Component layout and edge connector connections, AC04/1



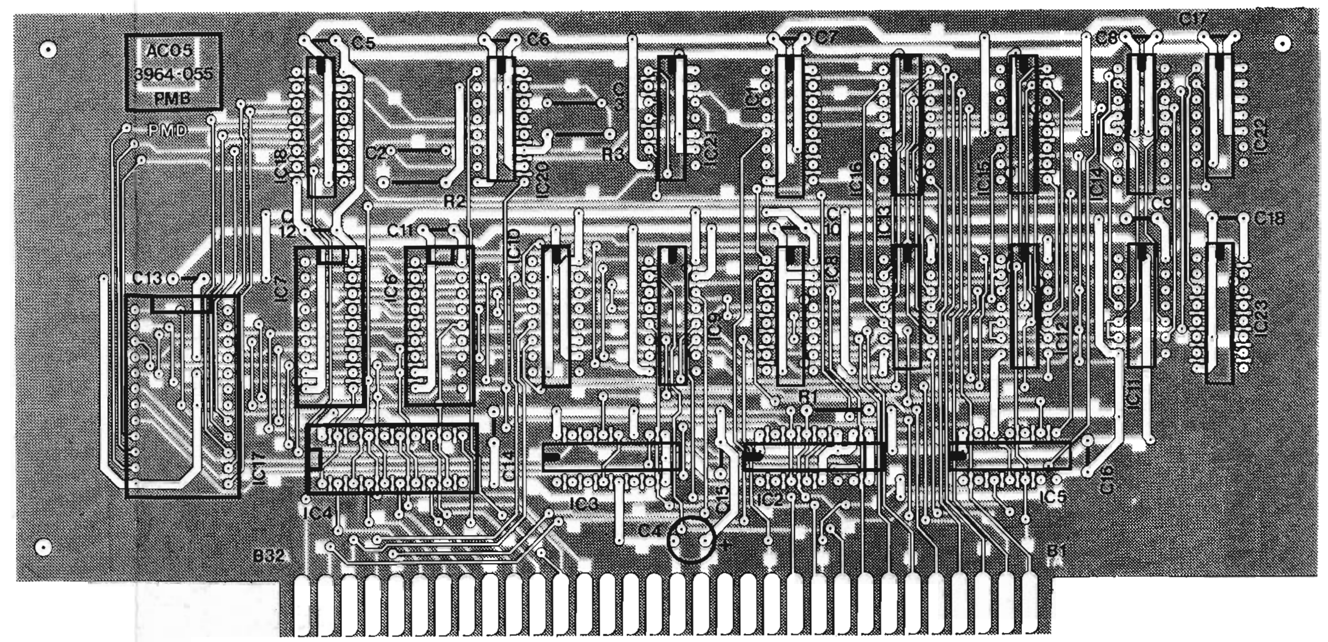
3964/929, Iss. 1

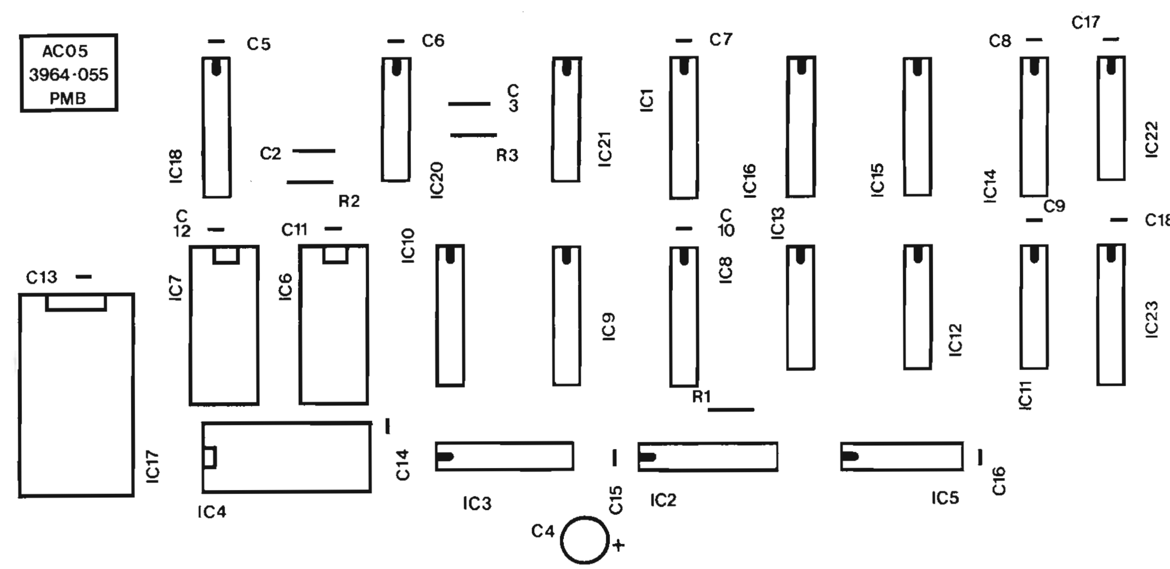
AC04/1

Fig. 3 Video circuit (graticule), AC04/1



EDGE CONNECTOR VIEWED
FROM UNDERSIDE OF
MOTHER BOARD





ACO5

Fig. 4a Component layout and edge connector connections, AC05

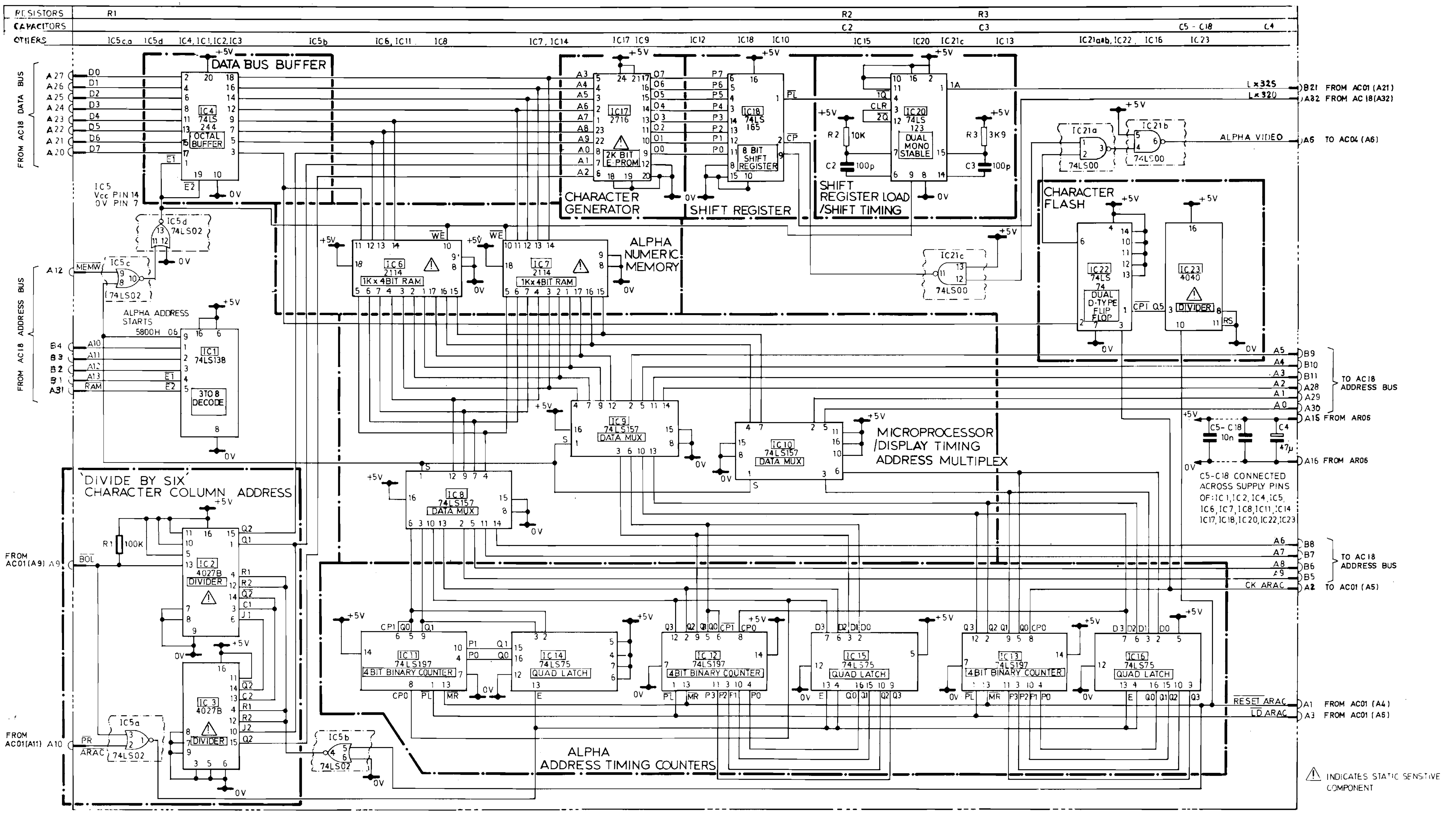
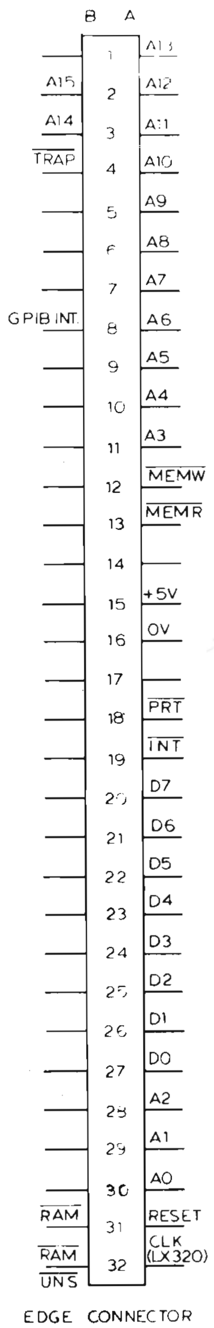
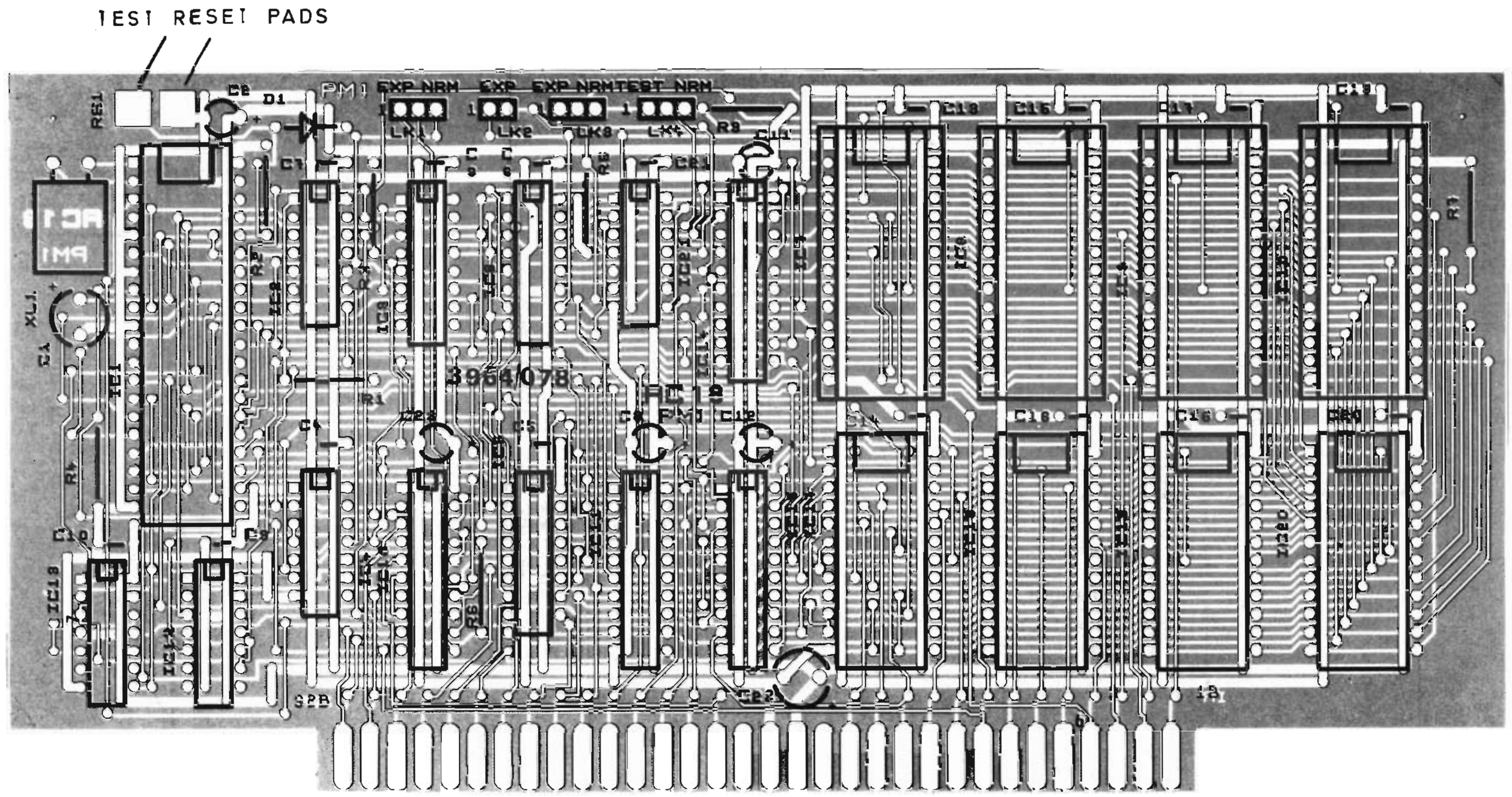
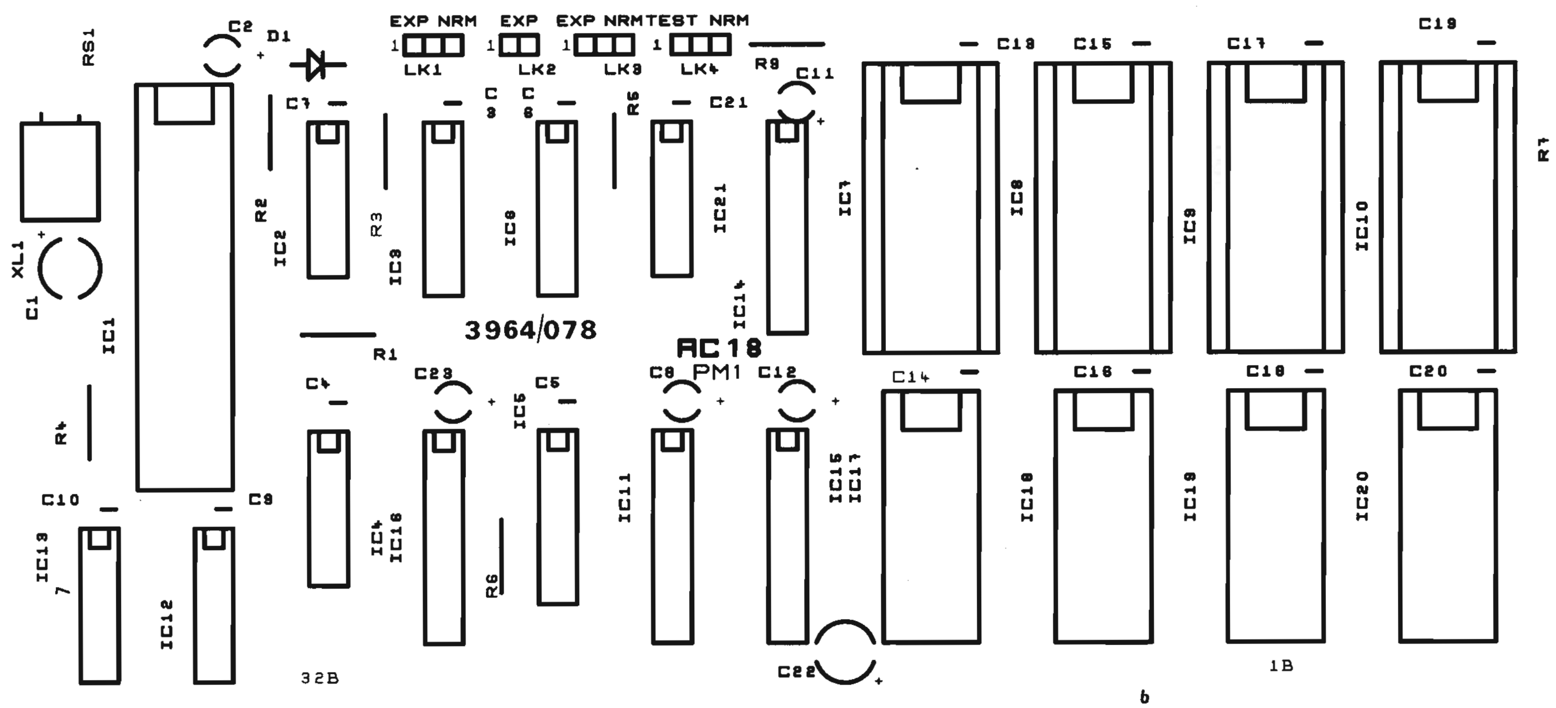


Fig. 4 Alpha generator, AC05

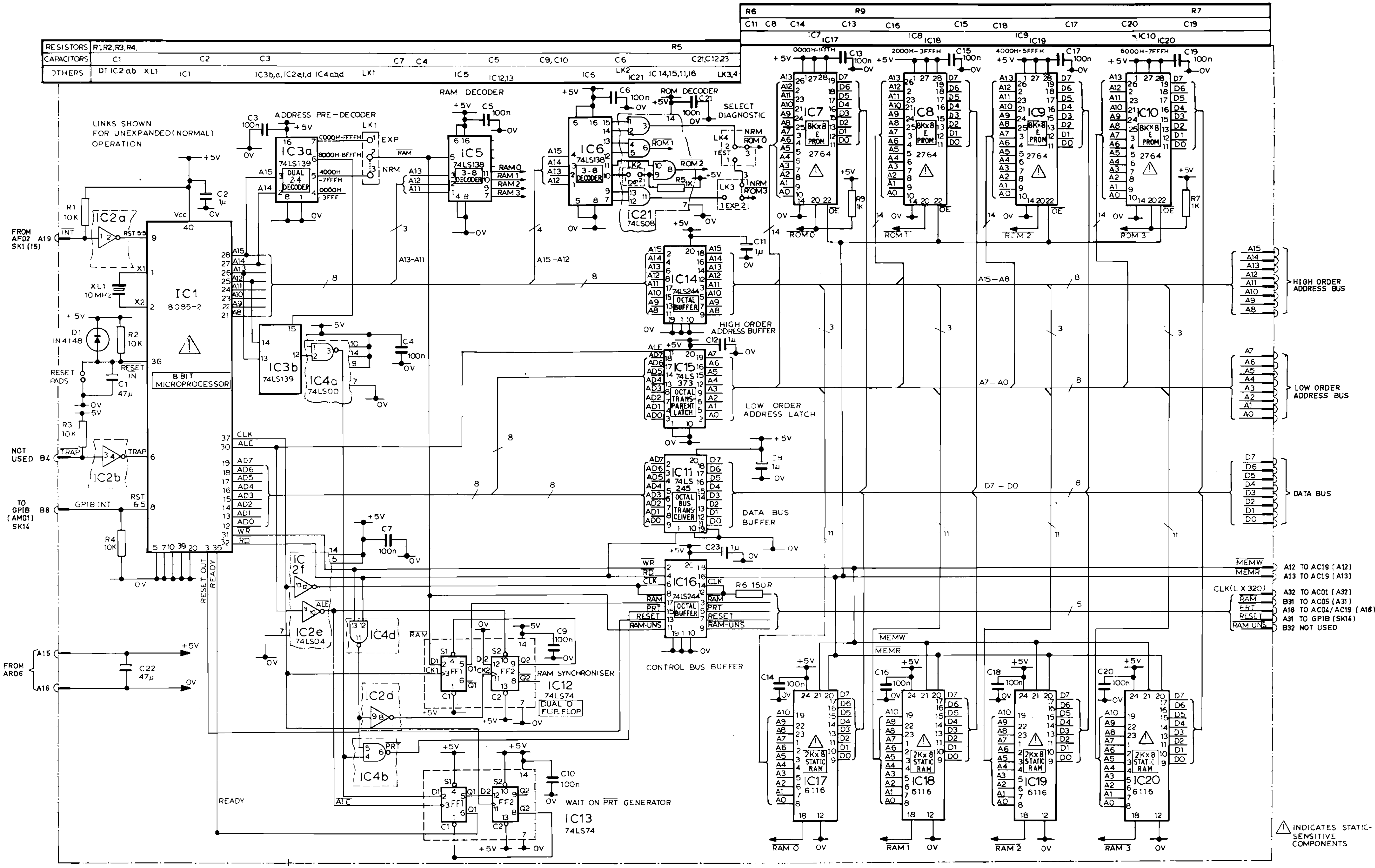






AC18

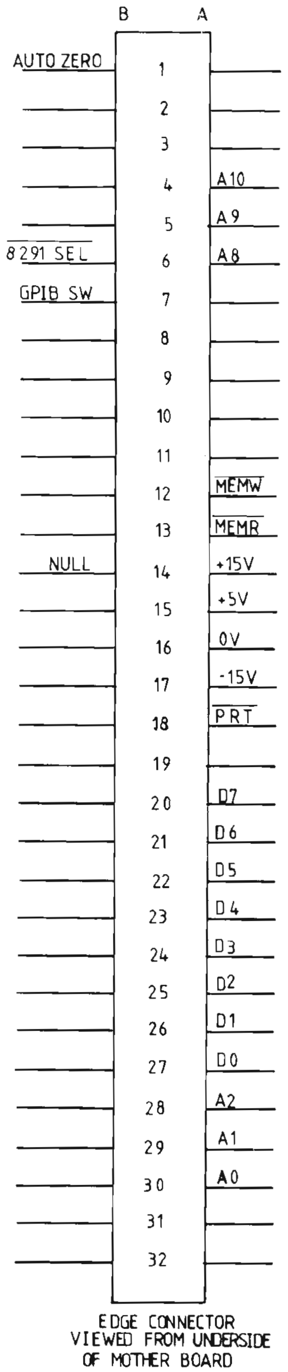
Fig. 5a Component layout and edge connector connections, AC18

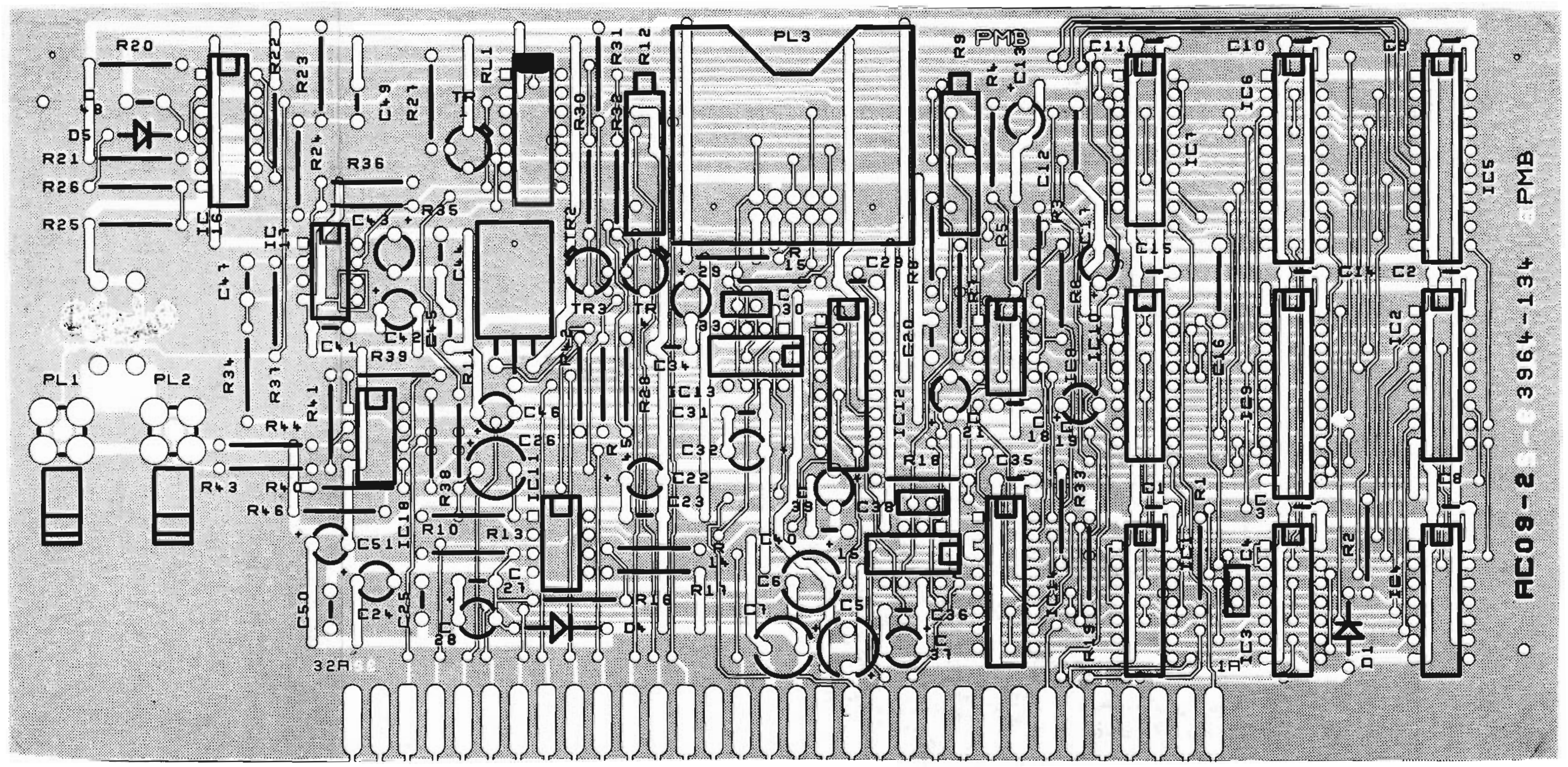


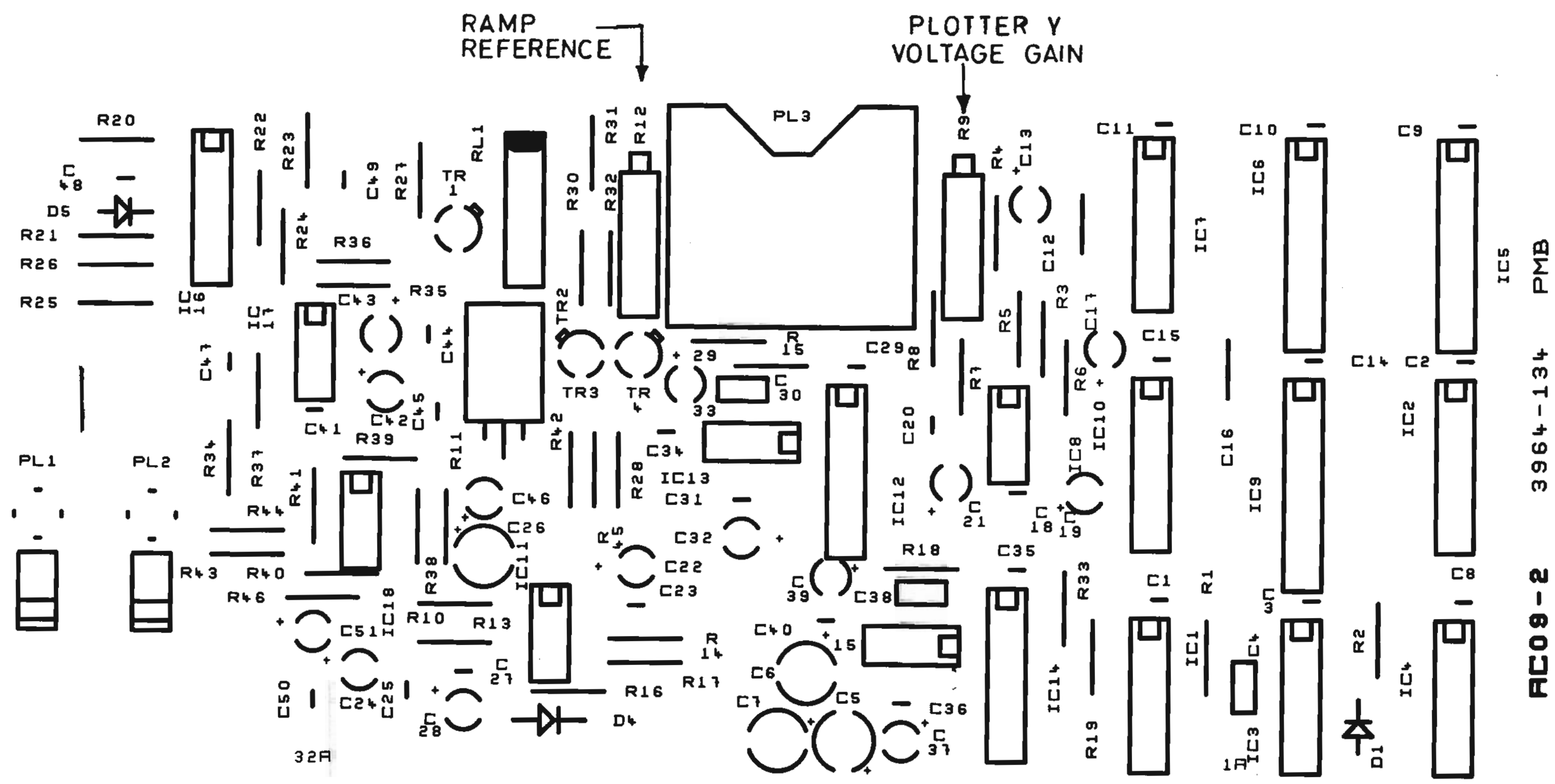
3964/923, Iss. 2

AC18

Fig. 5 Microprocessor, AC18

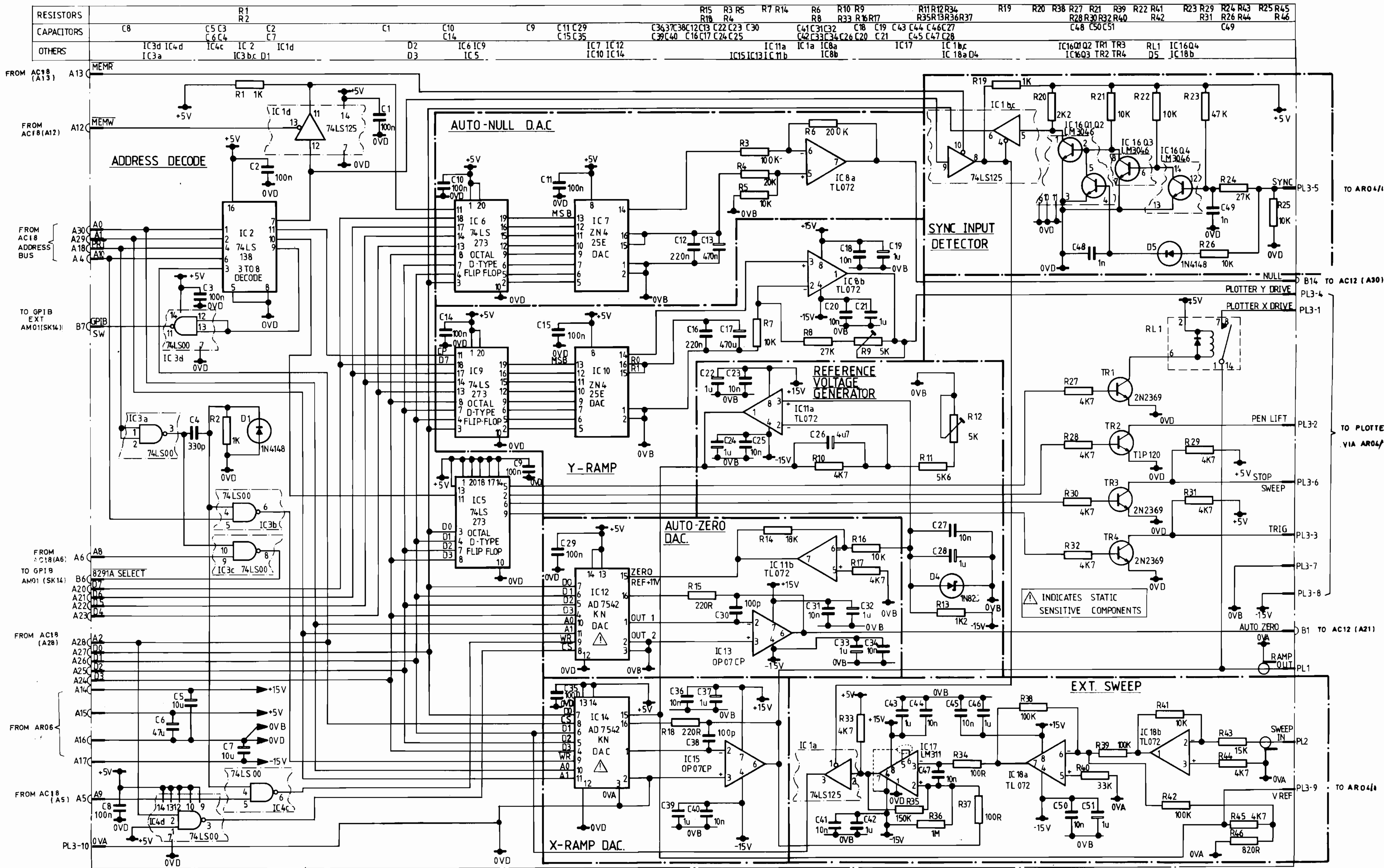






AC09/2

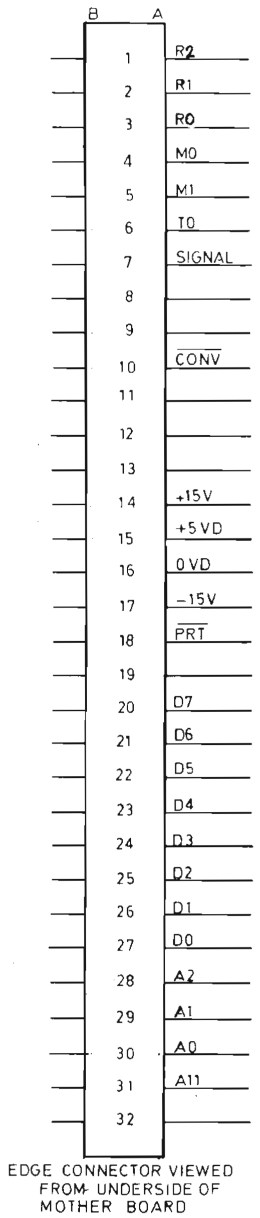
Fig. 6a Component layout and edge connector connections, AC09/2

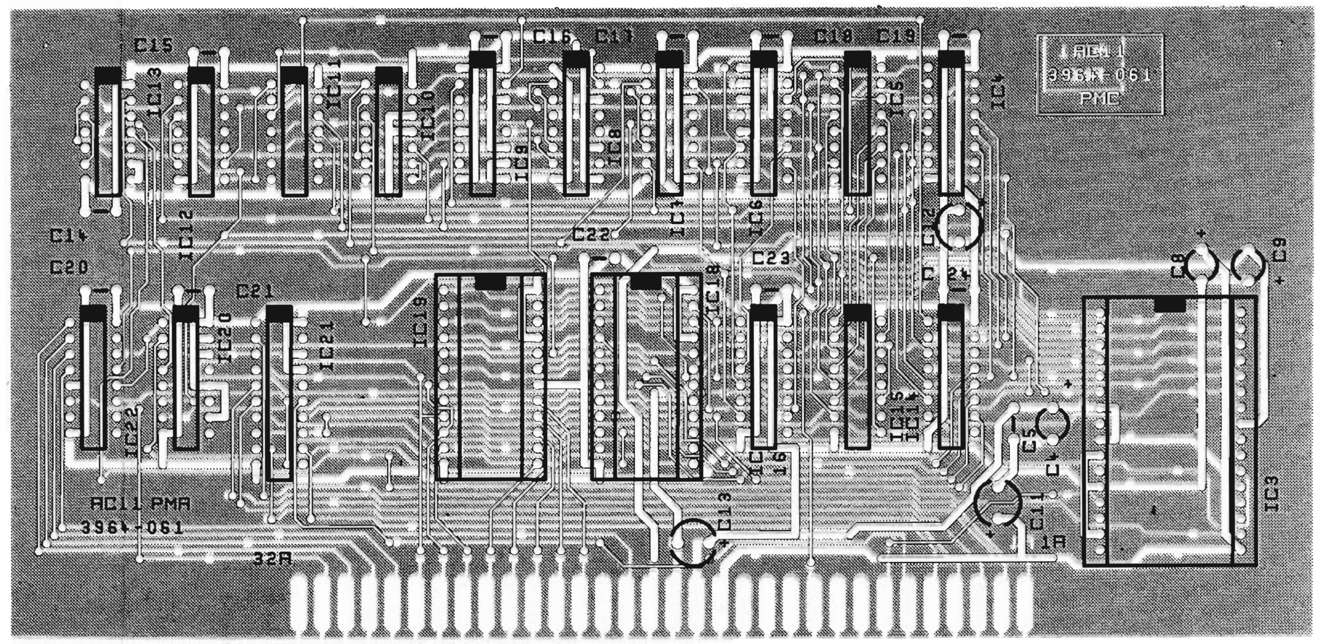


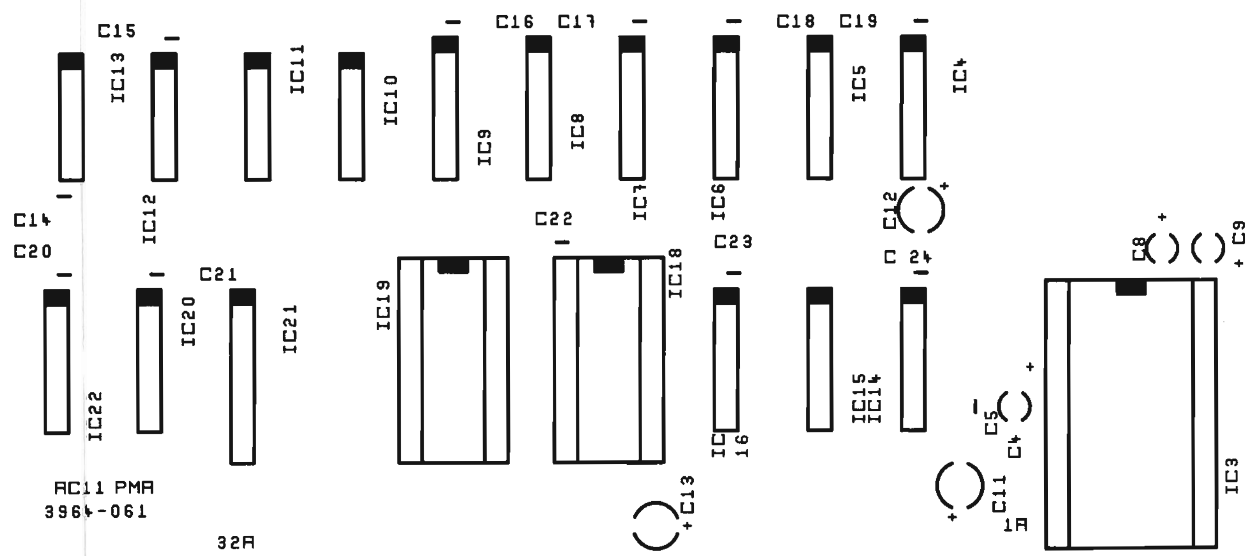
3964/927, Iss. 2

Fig. 6 In-Out (Port control), AC09/2

AC09/2

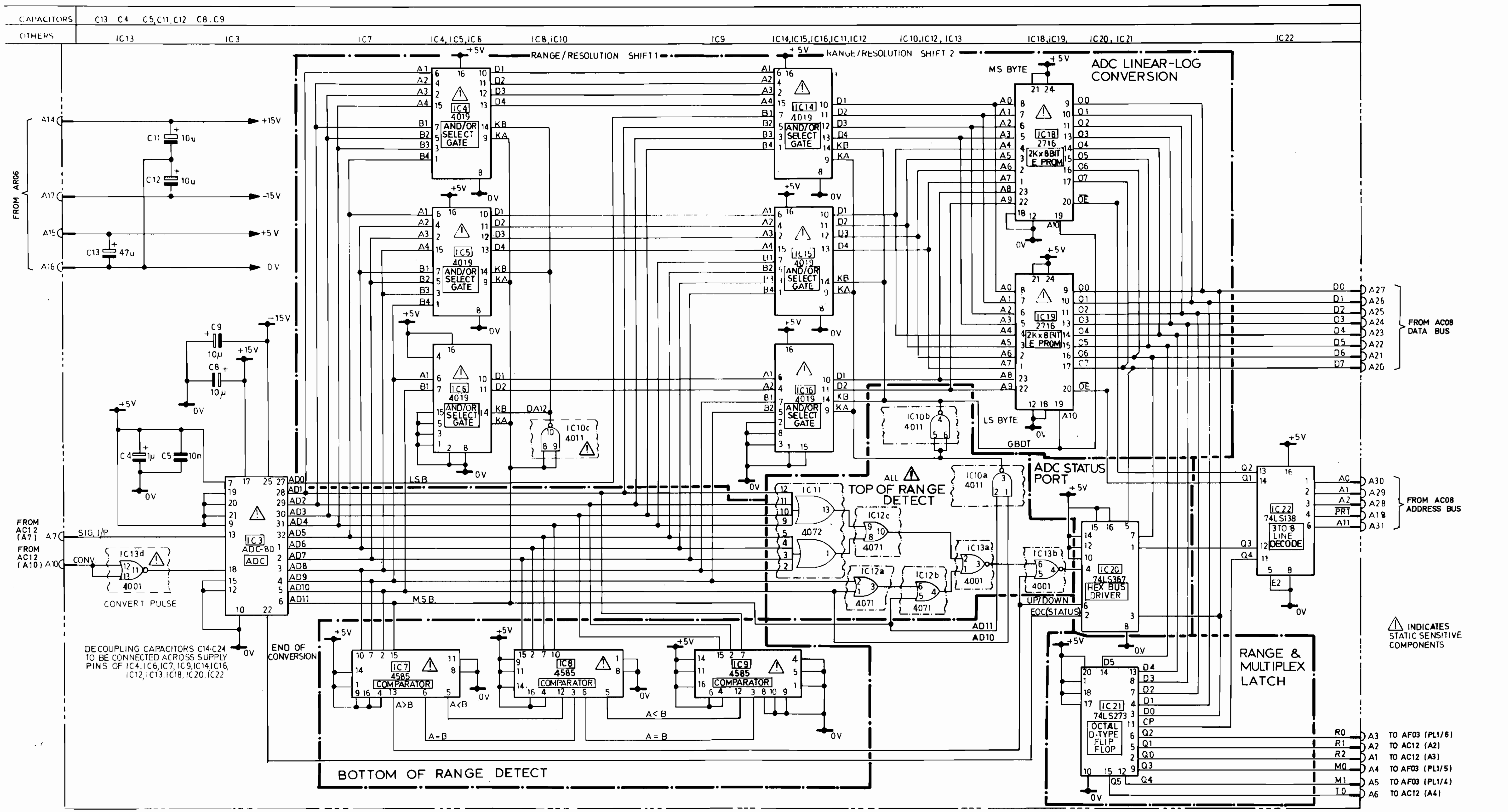






AC11

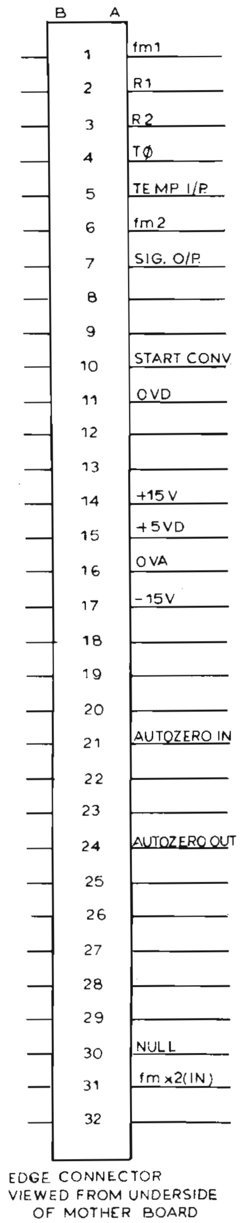
Fig. 7a Component layout and edge connector connections, AC11

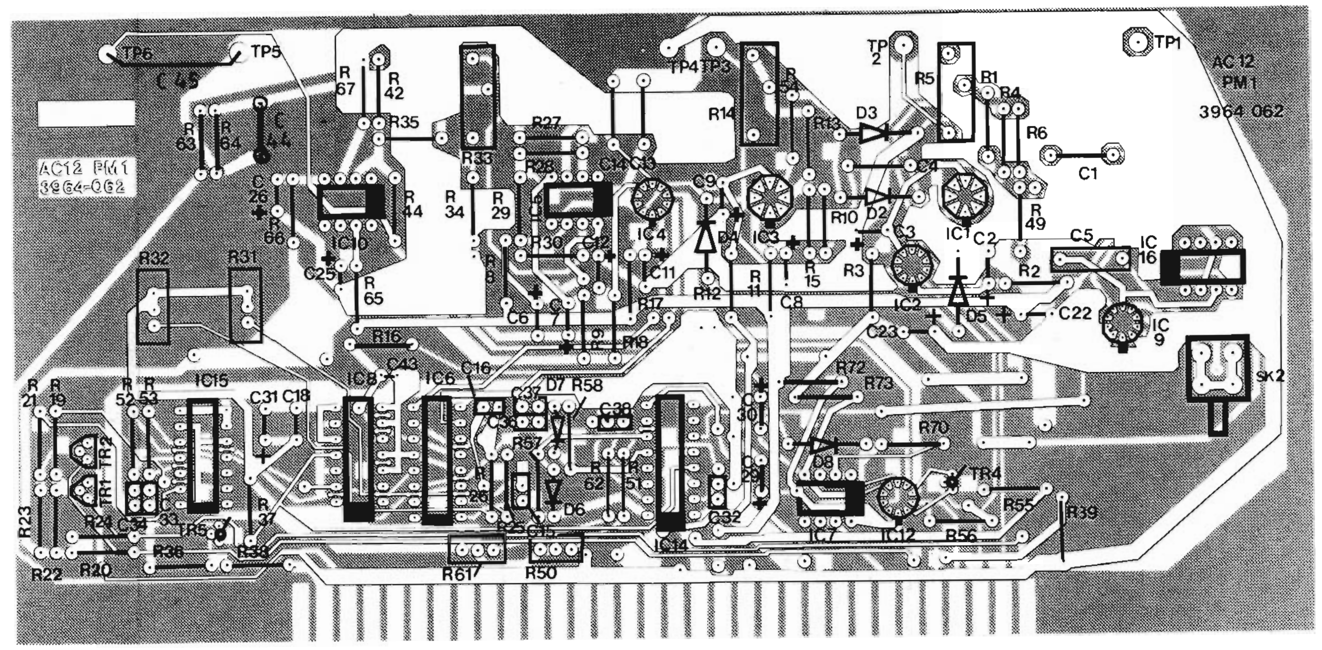


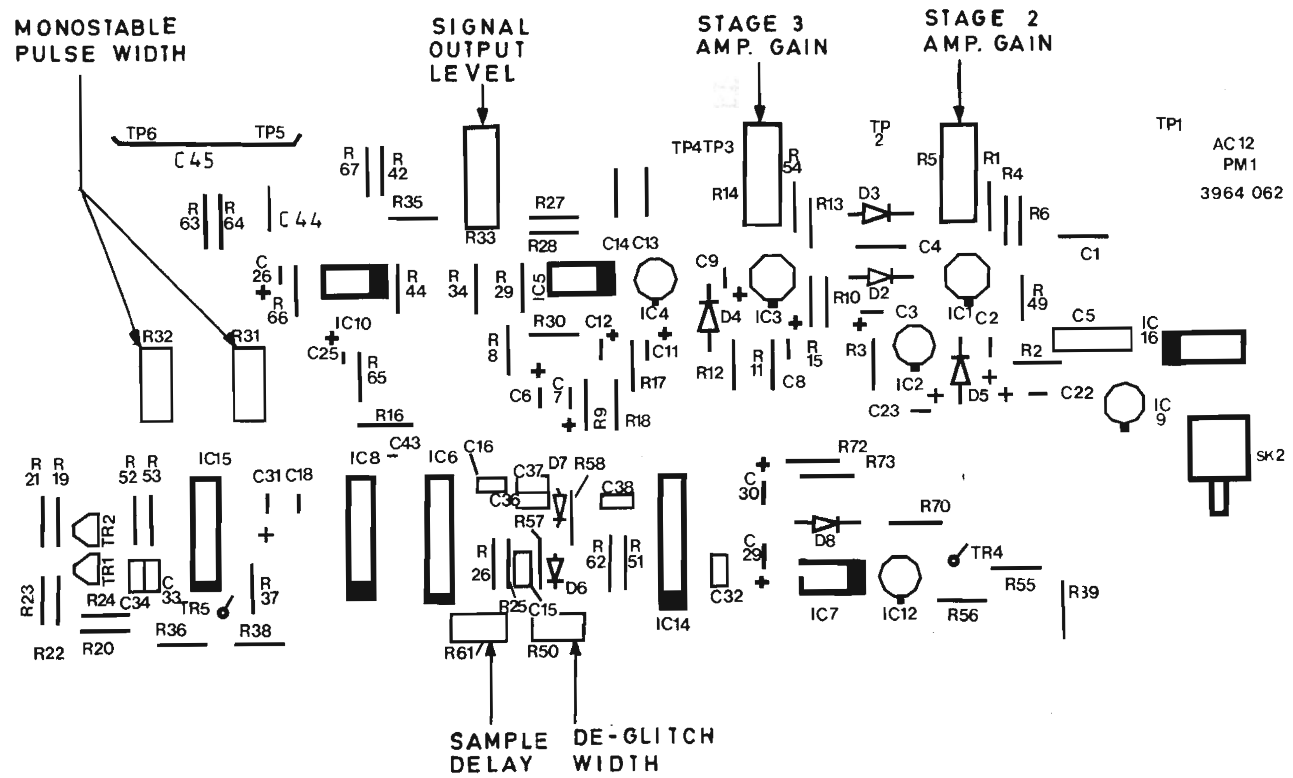
3964/911, Iss. 1

AC11

Fig. 7   A-D system and log conversion, AC11

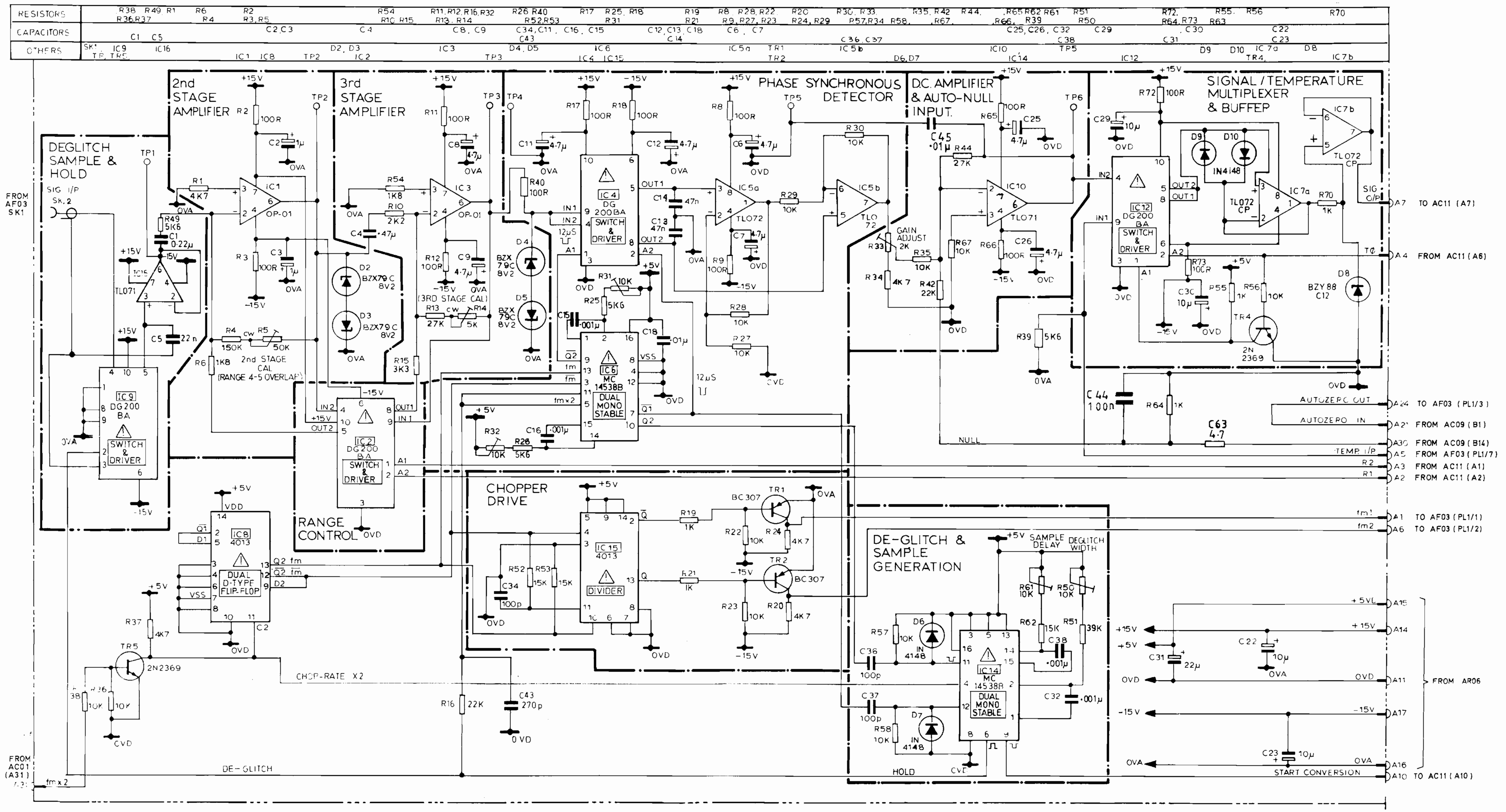






AC12

Fig. 8a Component layout and edge connector connections, AC12

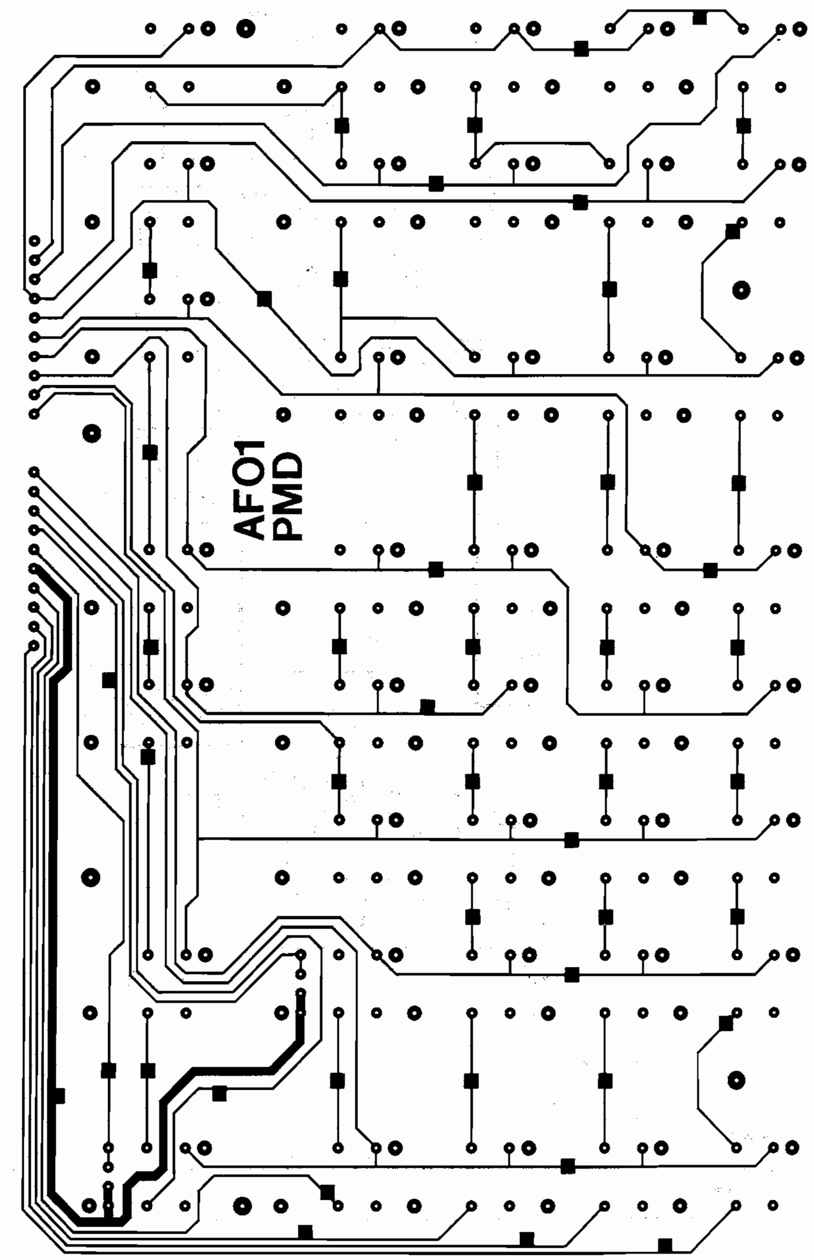


3964/912, Iss. 3

AC12

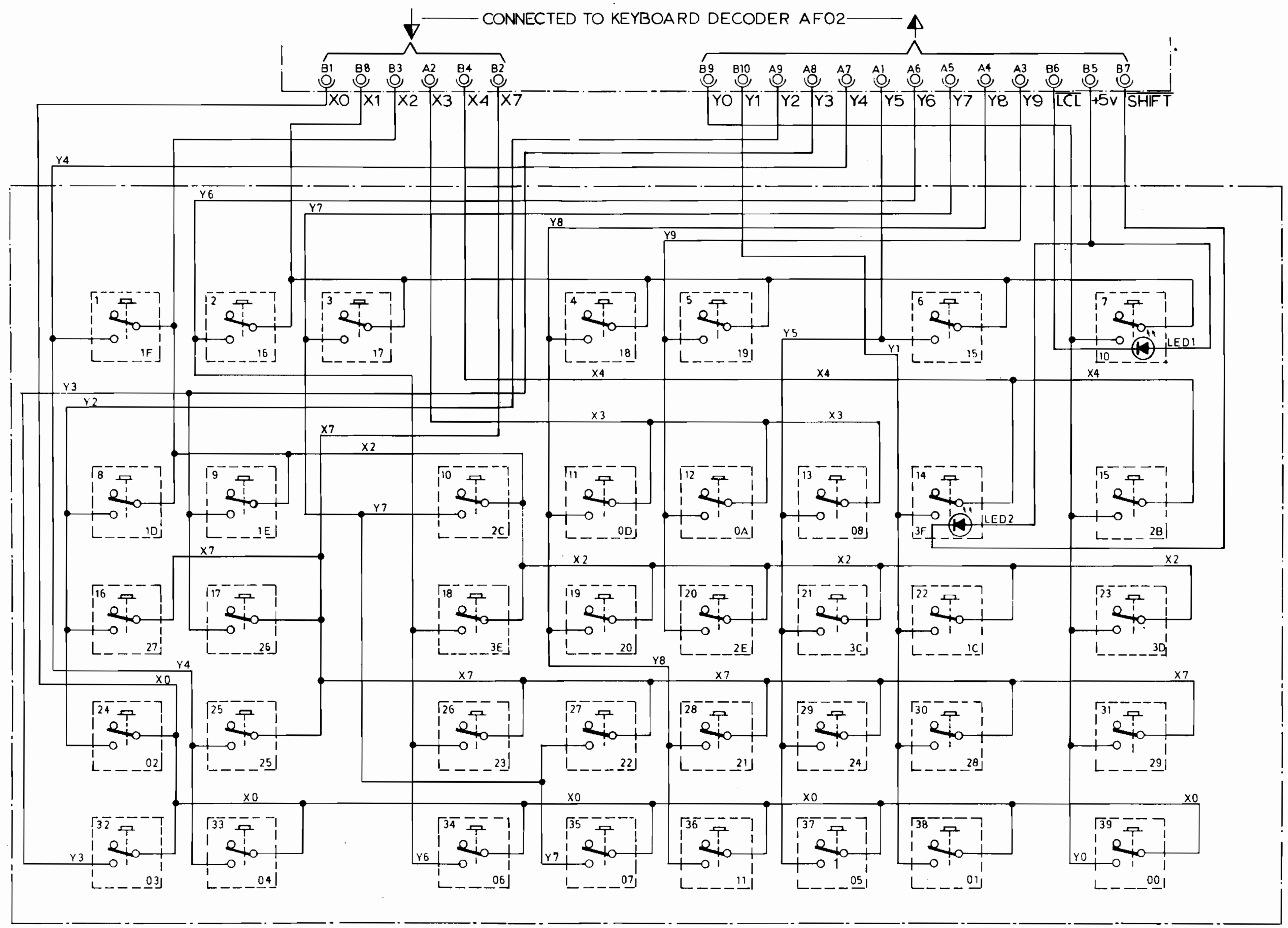
Fig. 8 Signal channel, AC12

KEY Nº	X	Y	CODE (HEX)
1	X2	Y4	1F
2	X1	Y6	16
3	X1	Y7	17
4	X1	Y8	18
5	X1	Y9	19
6	X1	Y5	15
7	X1	Y0	10
8	X2	Y2	1D
9	X2	Y3	1E
10	X2	Y7	2C
11	X3	Y8	0D
12	X3	Y9	0A
13	X3	Y5	08
14	X4	Y1	3F
15	X4	Y0	2B
16	X7	Y2	27
17	X7	Y3	26
18	X2	Y6	3E
19	X2	Y8	20
20	X2	Y9	2E
21	X2	Y5	3C
22	X2	Y1	1C
23	X2	Y0	3D
24	X0	Y2	02
25	X7	Y4	25
26	X7	Y6	23
27	X7	Y7	22
28	X7	Y8	21
29	X7	Y5	24
30	X7	Y1	28
31	X7	Y0	29
32	X0	Y3	03
33	X0	Y4	04
34	X0	Y6	06
35	X0	Y7	07
36	X0	Y8	11
37	X0	Y5	05
38	X0	Y1	01
39	X0	Y0	00



AF01

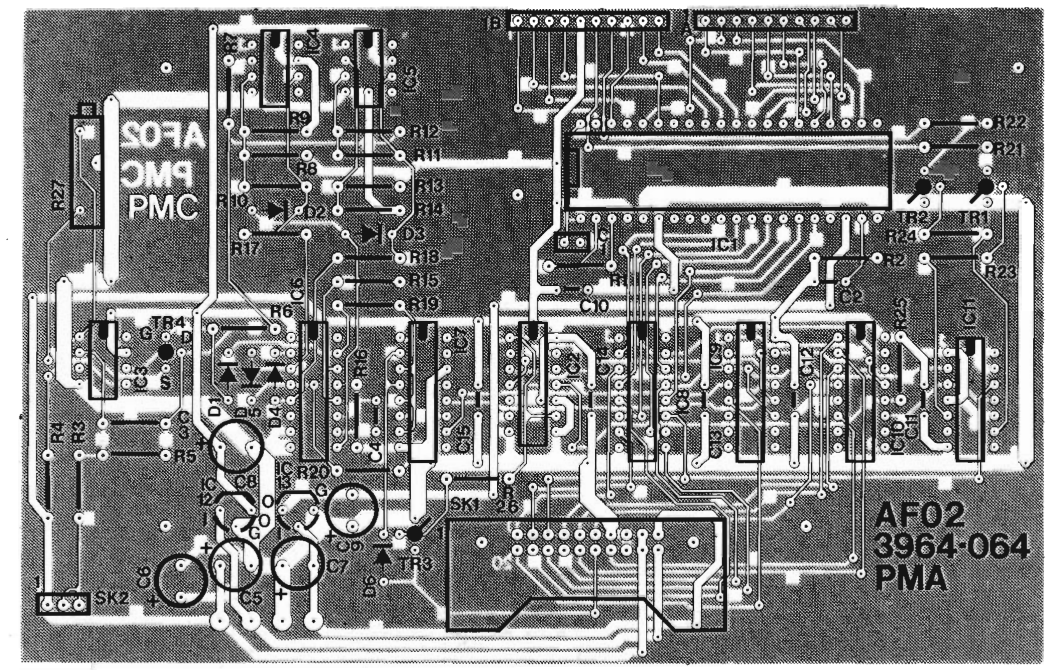
Fig. 9a Keyboard layout and key identification lines, AF01

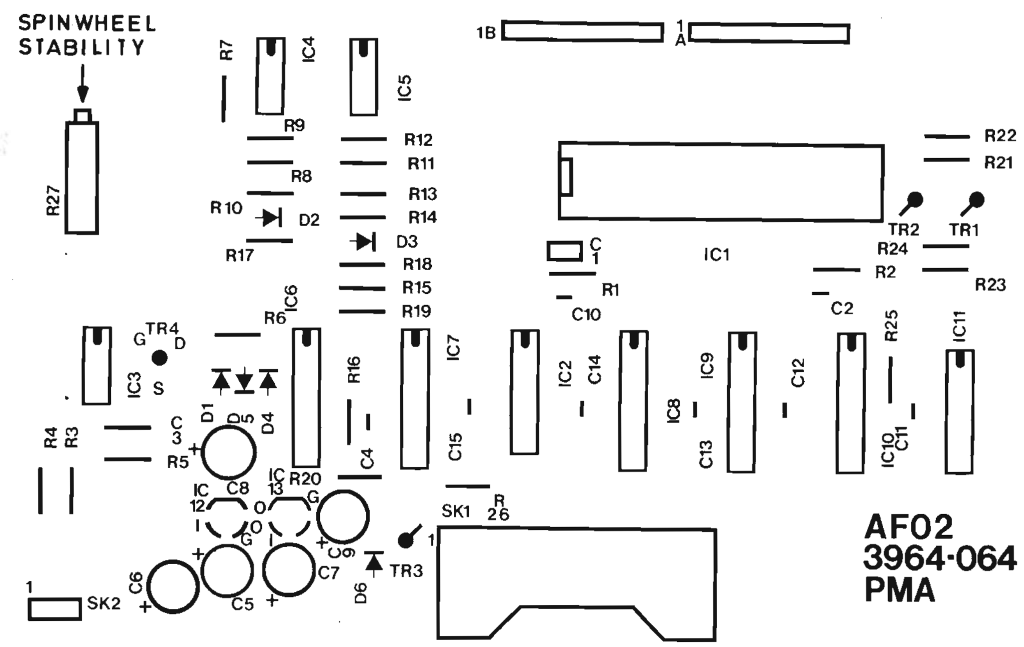


3964/913, Iss. 2

AF01

Fig. 9 Keyboard, AF01

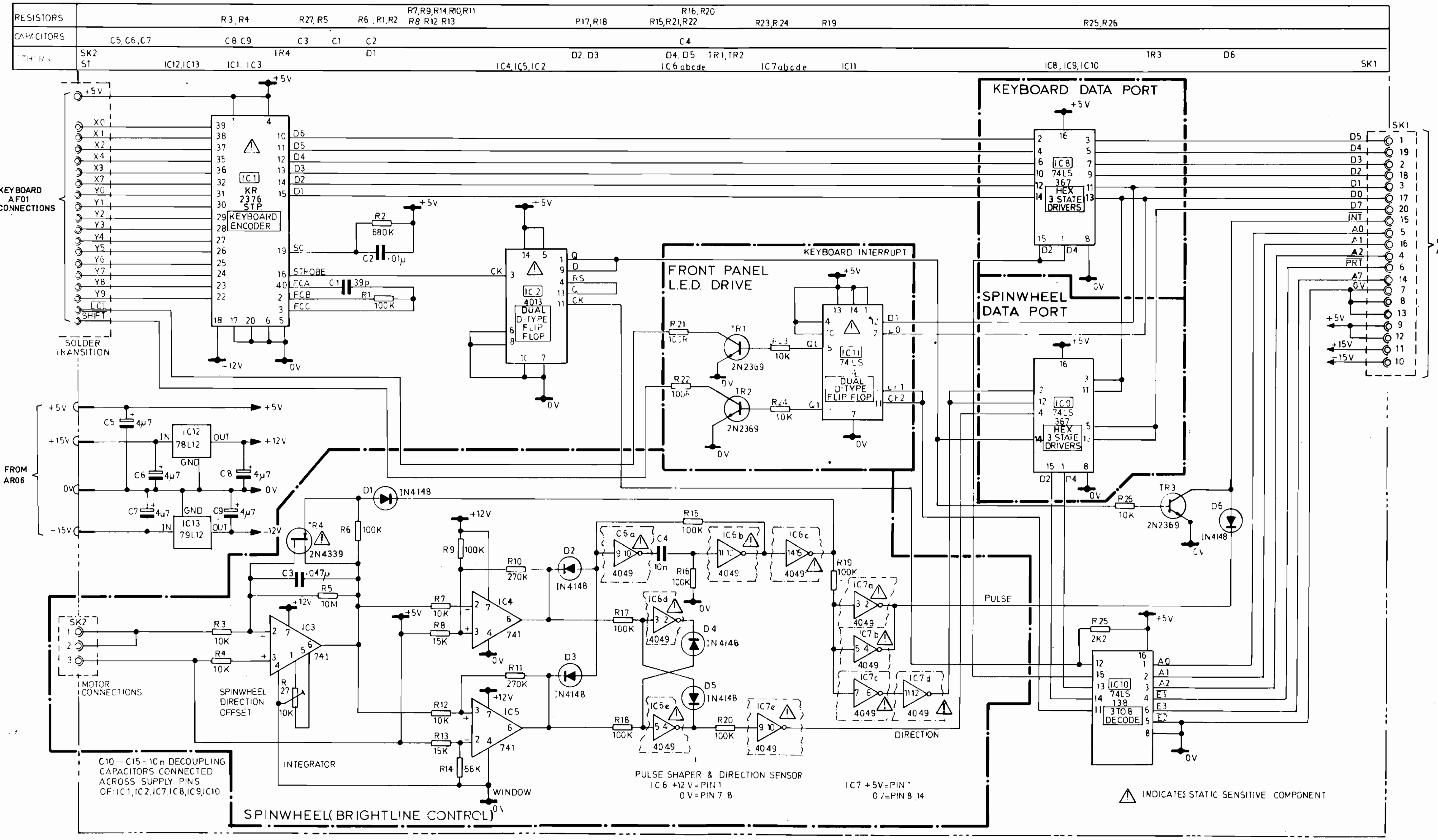




AF02

Fig. 10a Component layout, AF02

Fig. 10a



3964/914, Iss. 2

AF02

Fig. 10

Fig. 10 Keyboard decoder, AF02

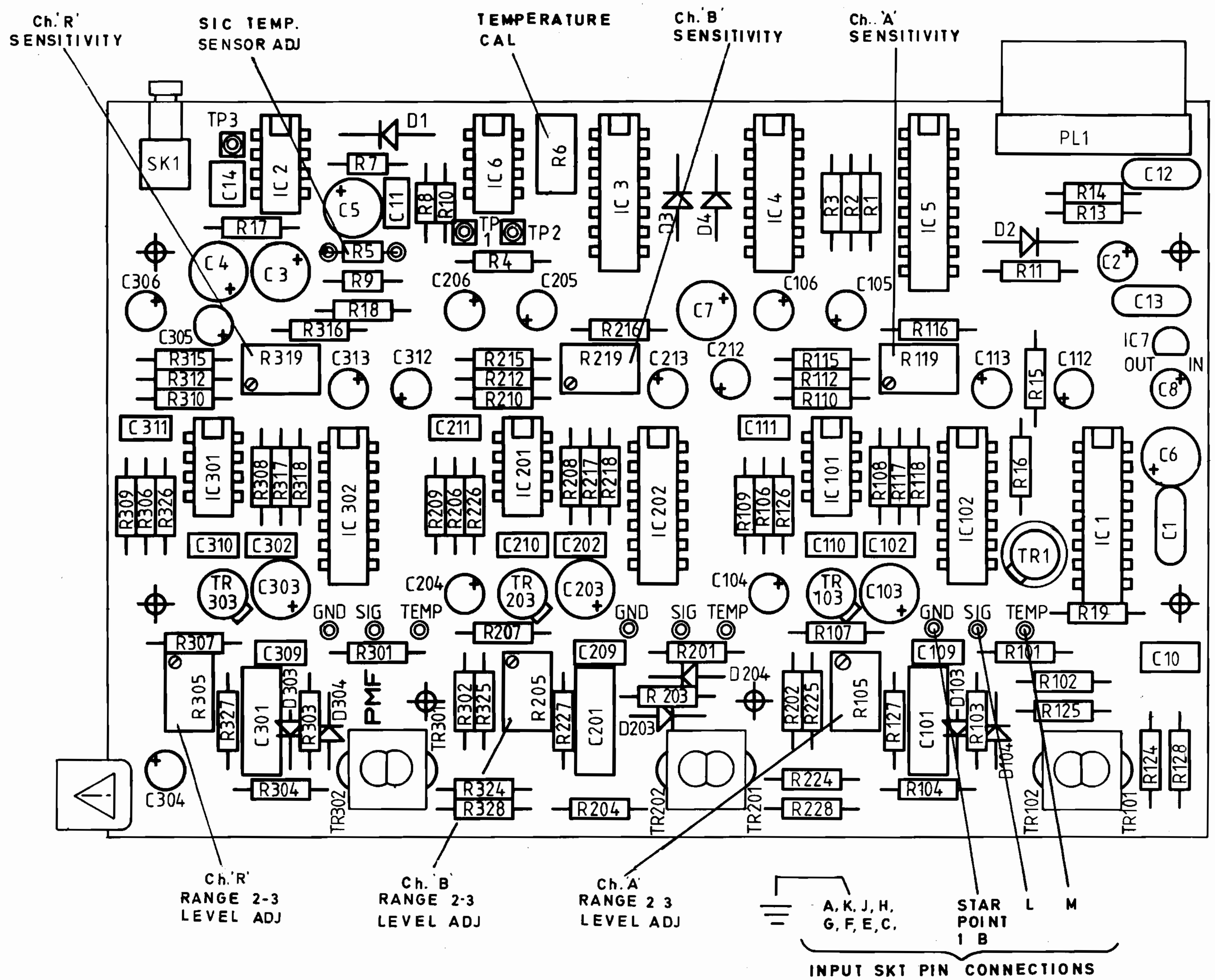
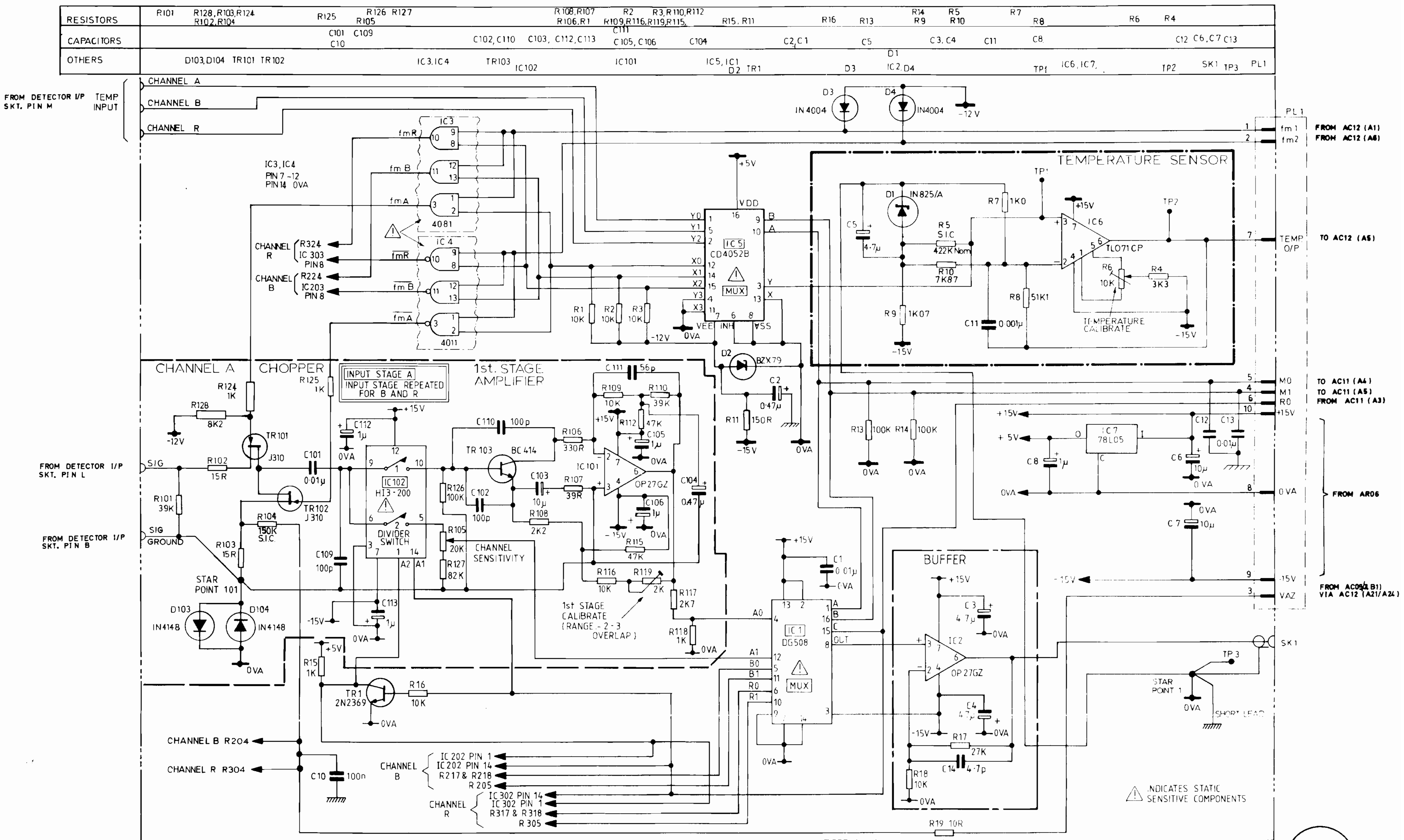


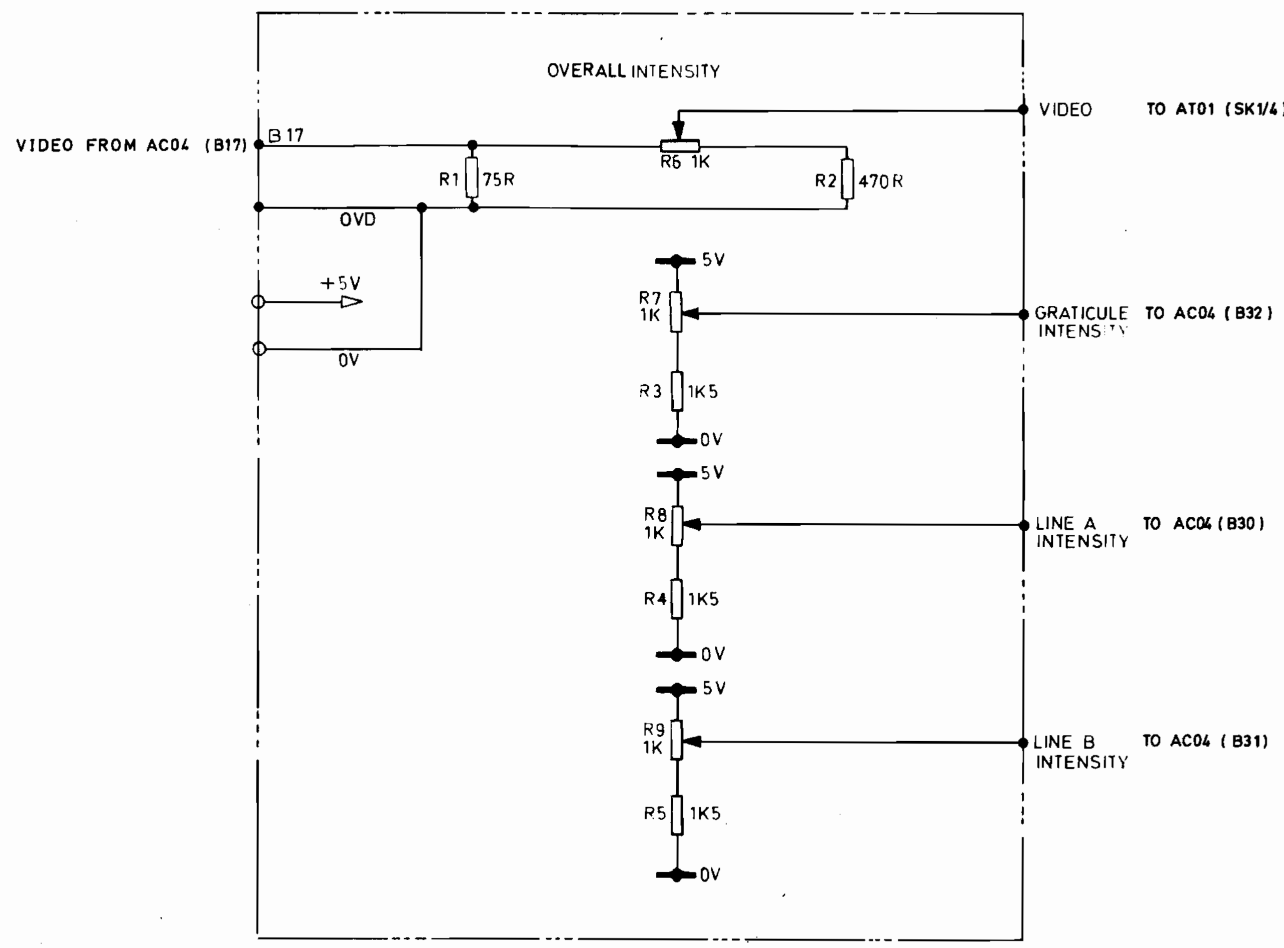
Fig. 11a Component layout, AF03/1



AF03/1

3964/926 Iss. 3

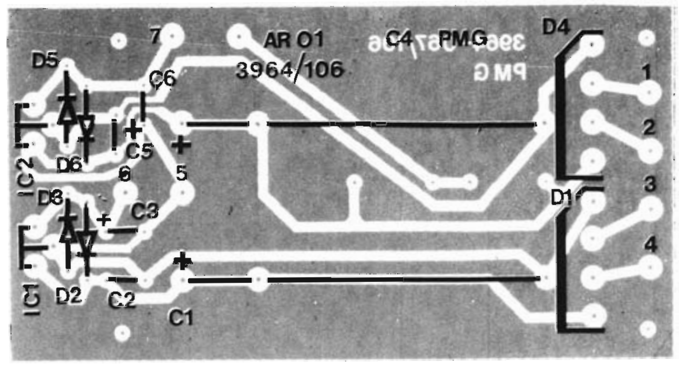
Fig. 11 Signal input board, AF03/1

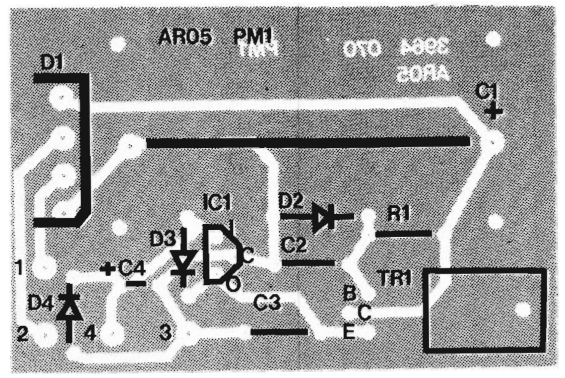


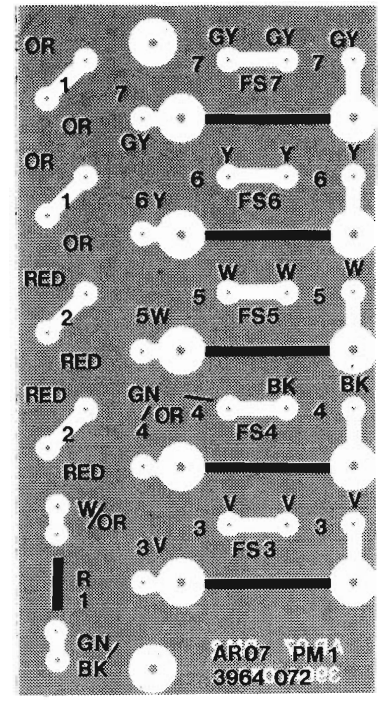
3964/922, Iss. 1

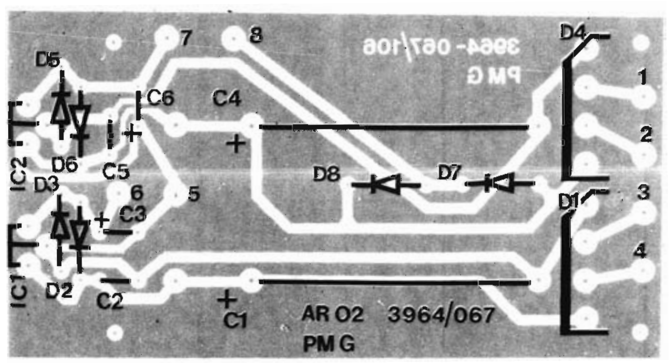
AF04

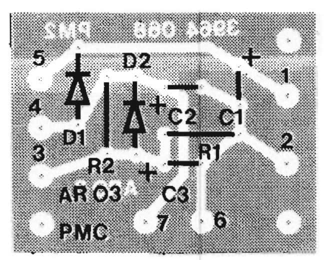
Fig. 12 Intensity control, AF04

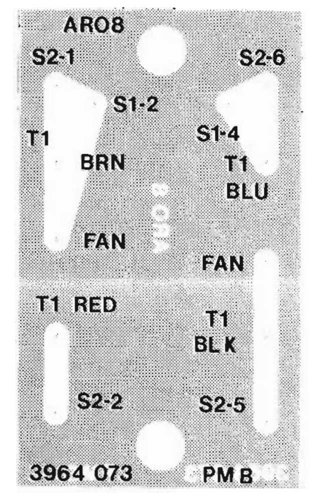






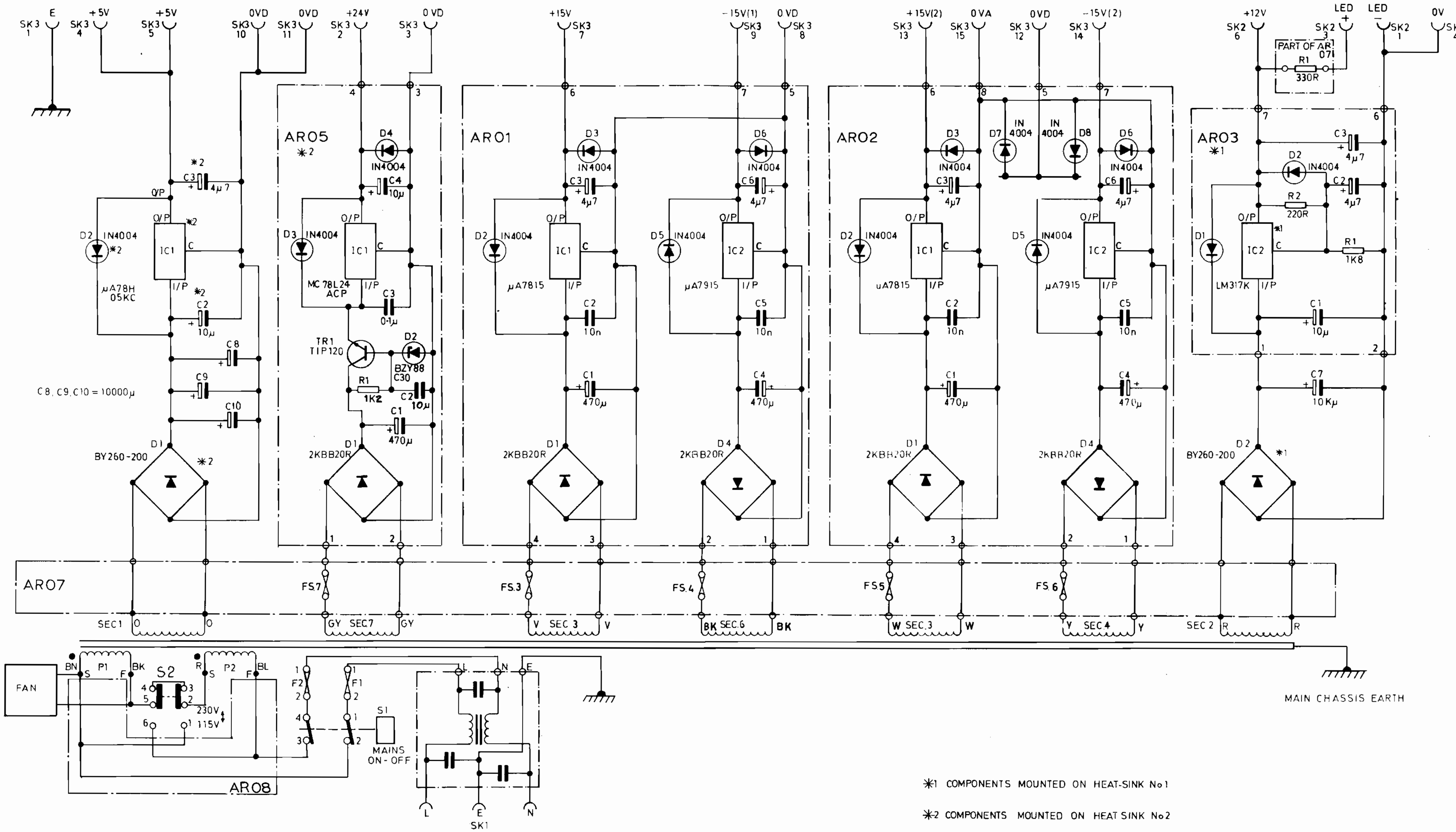






AR06

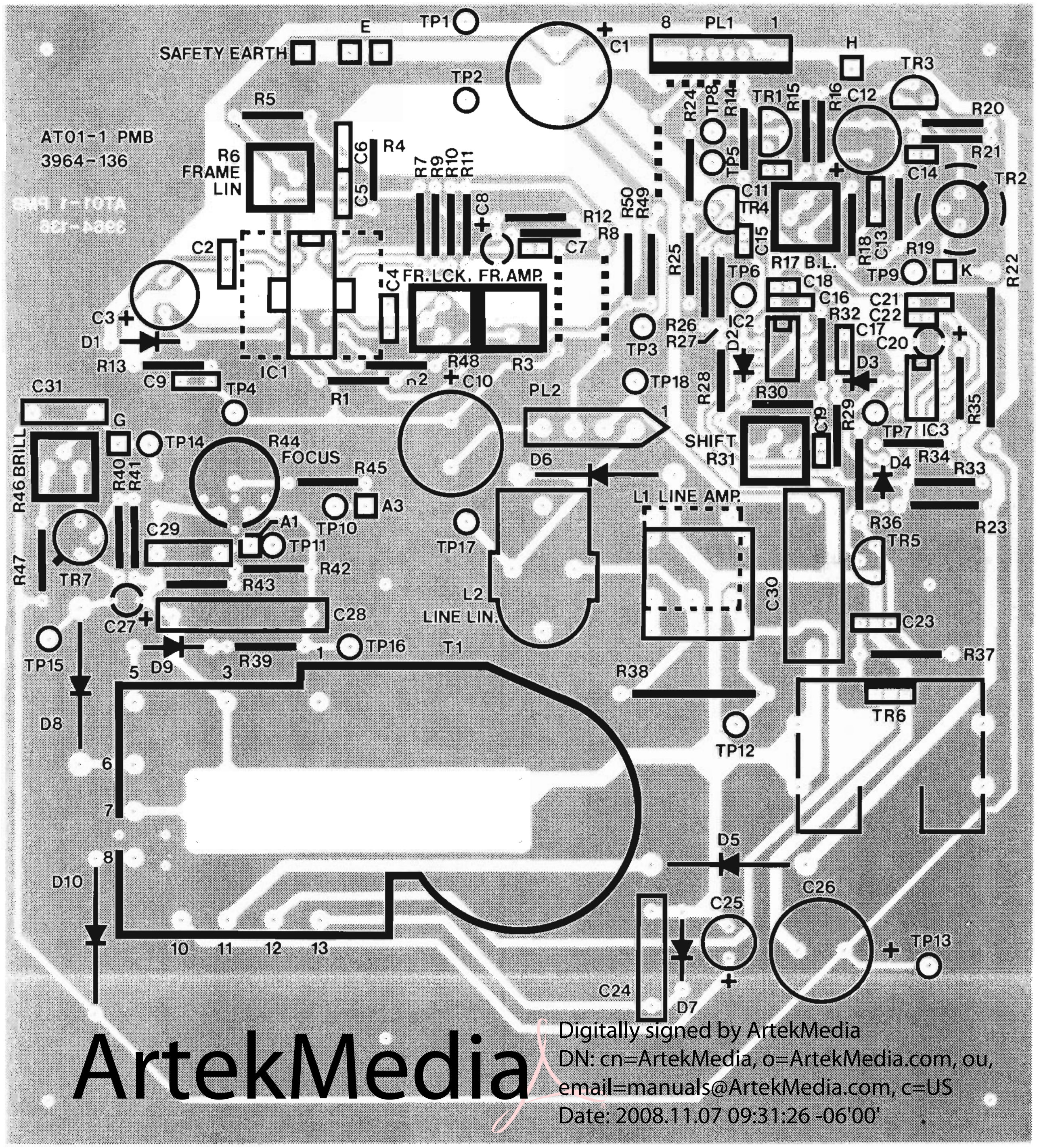
Fig. 13a Component layout, AR06 (AR01,AR02,AR03,AR05,AR07,AR08)



3964/916, Iss.3

AR06

Fig. 13 Power supply unit, AR06



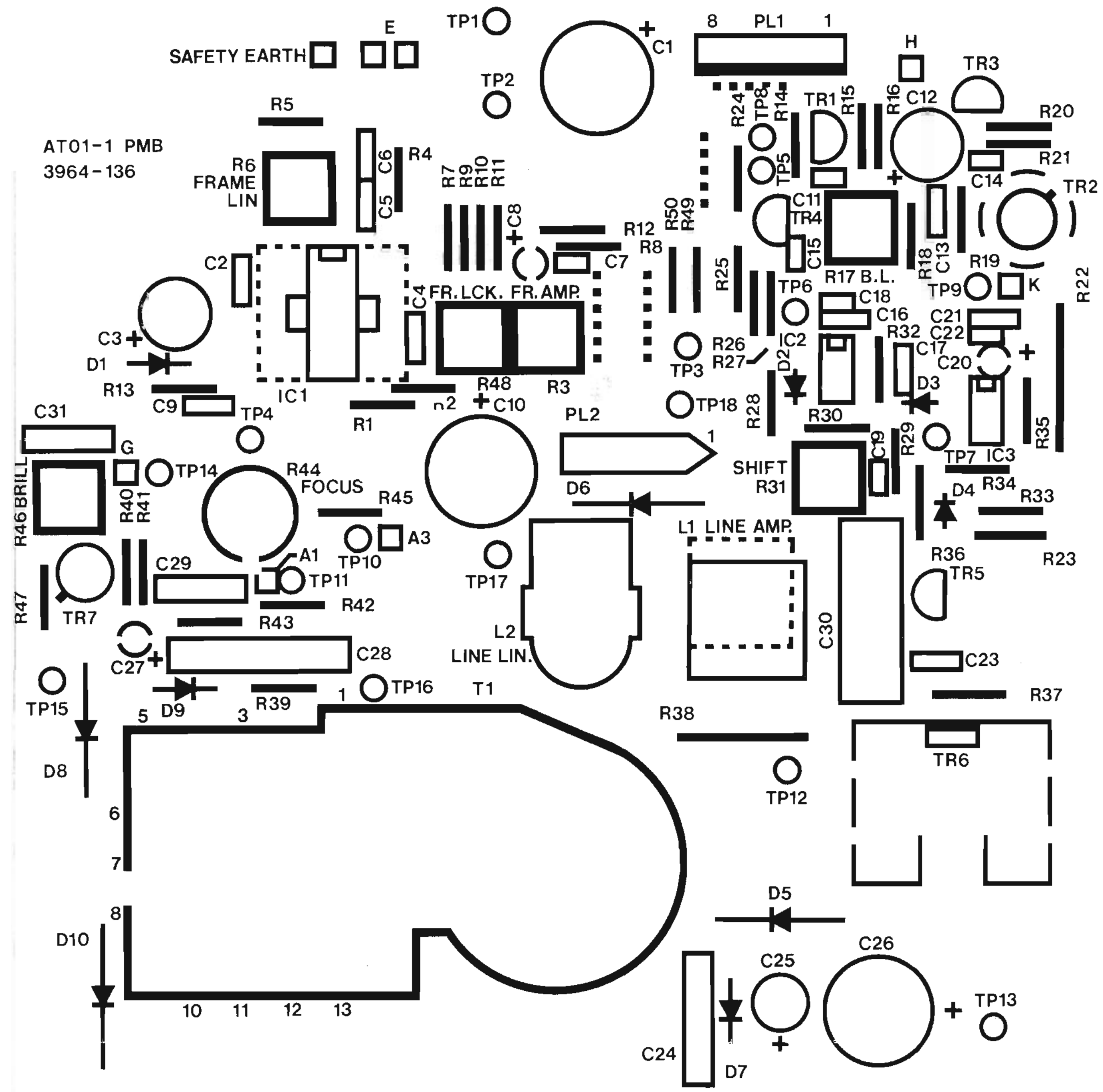
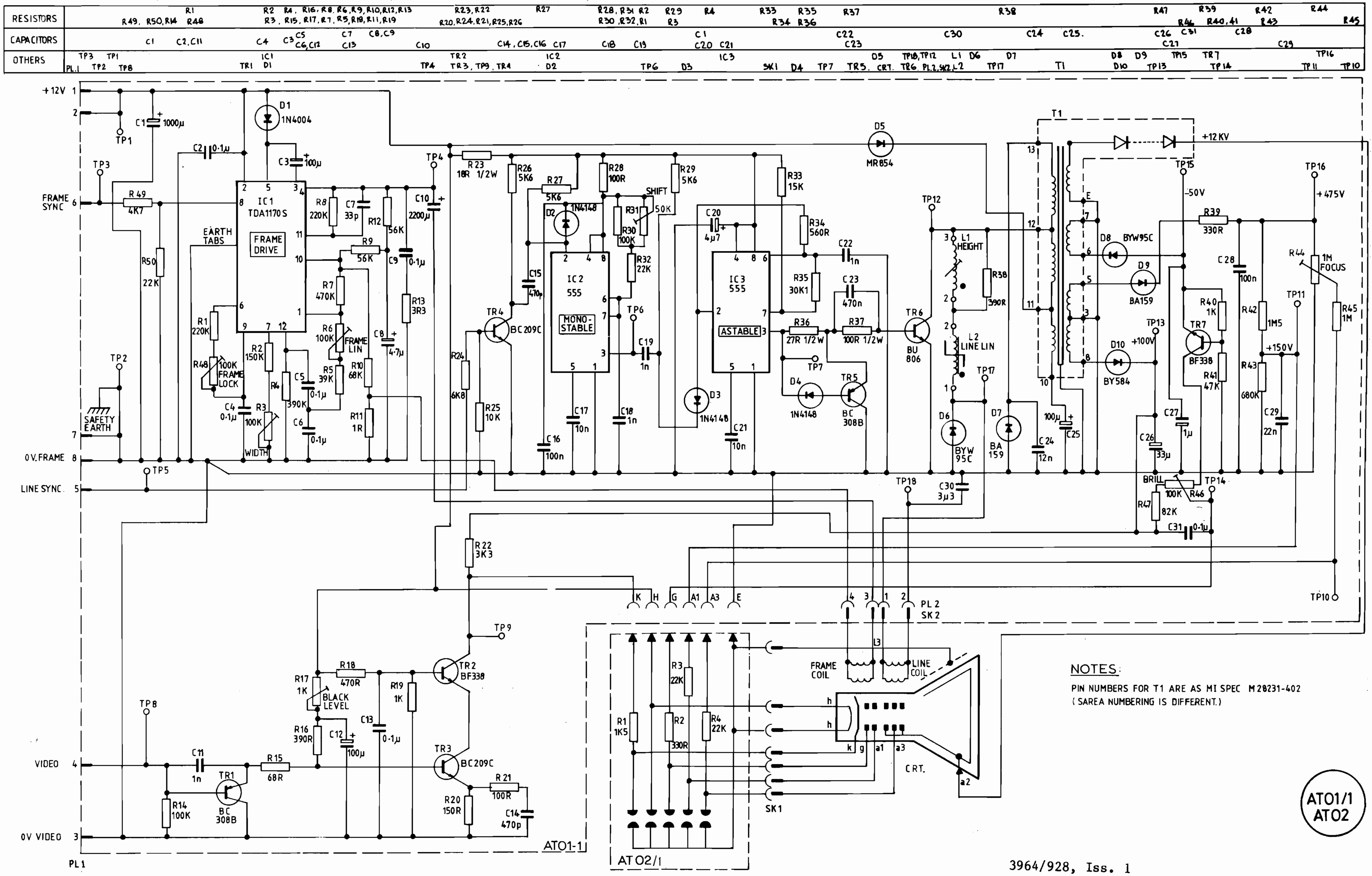
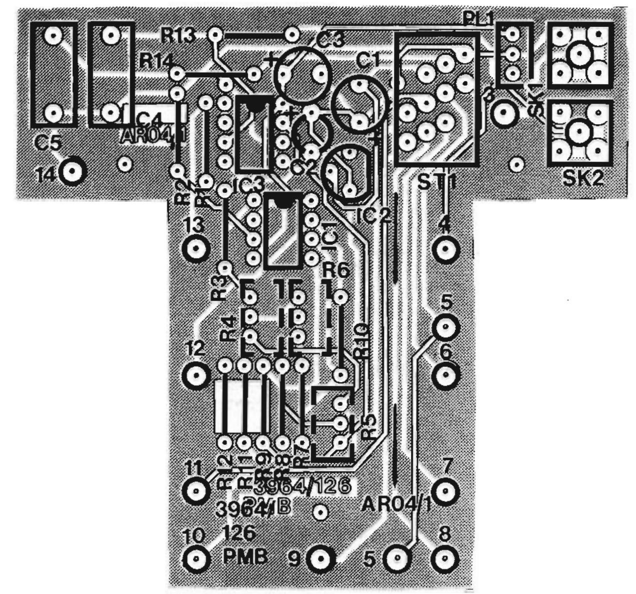


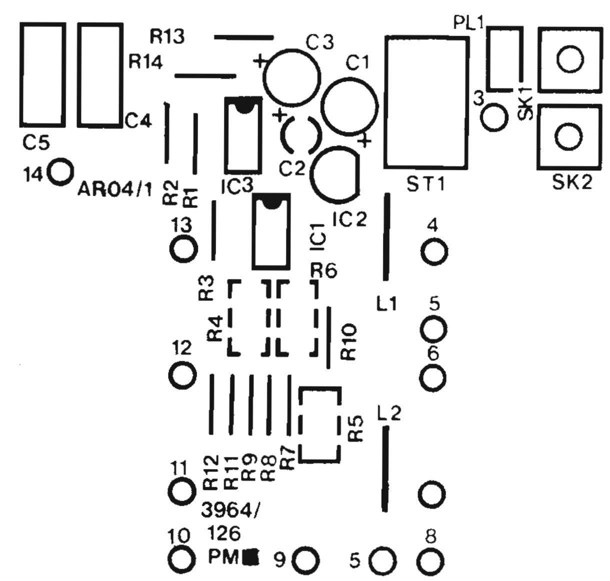
Fig. 14a Component layout, AT01/1



3964/928, Iss. 1

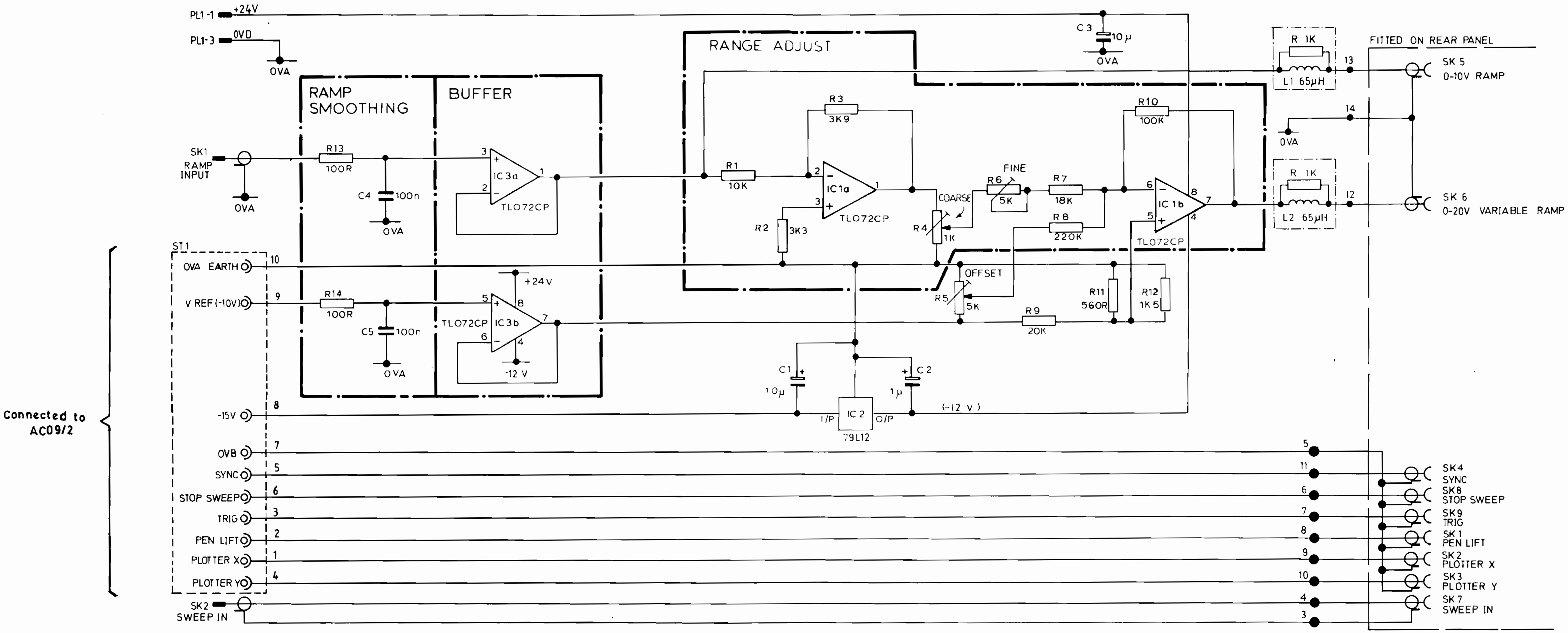
Fig. 14 CRT, AT01/1, AT02





AR04/1

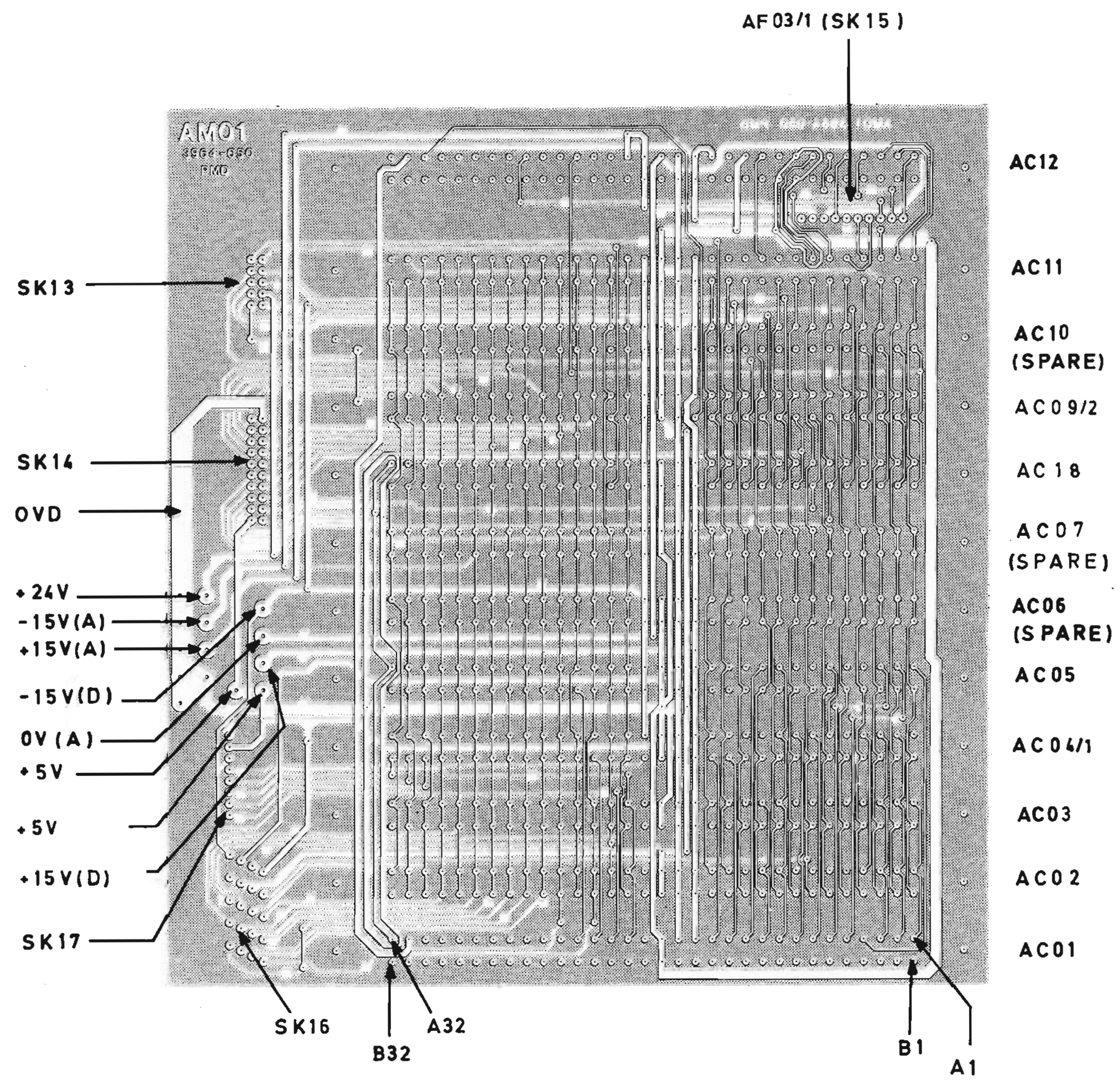
Fig. 15a Component layout, AR04/1



3964/925, Iss.1

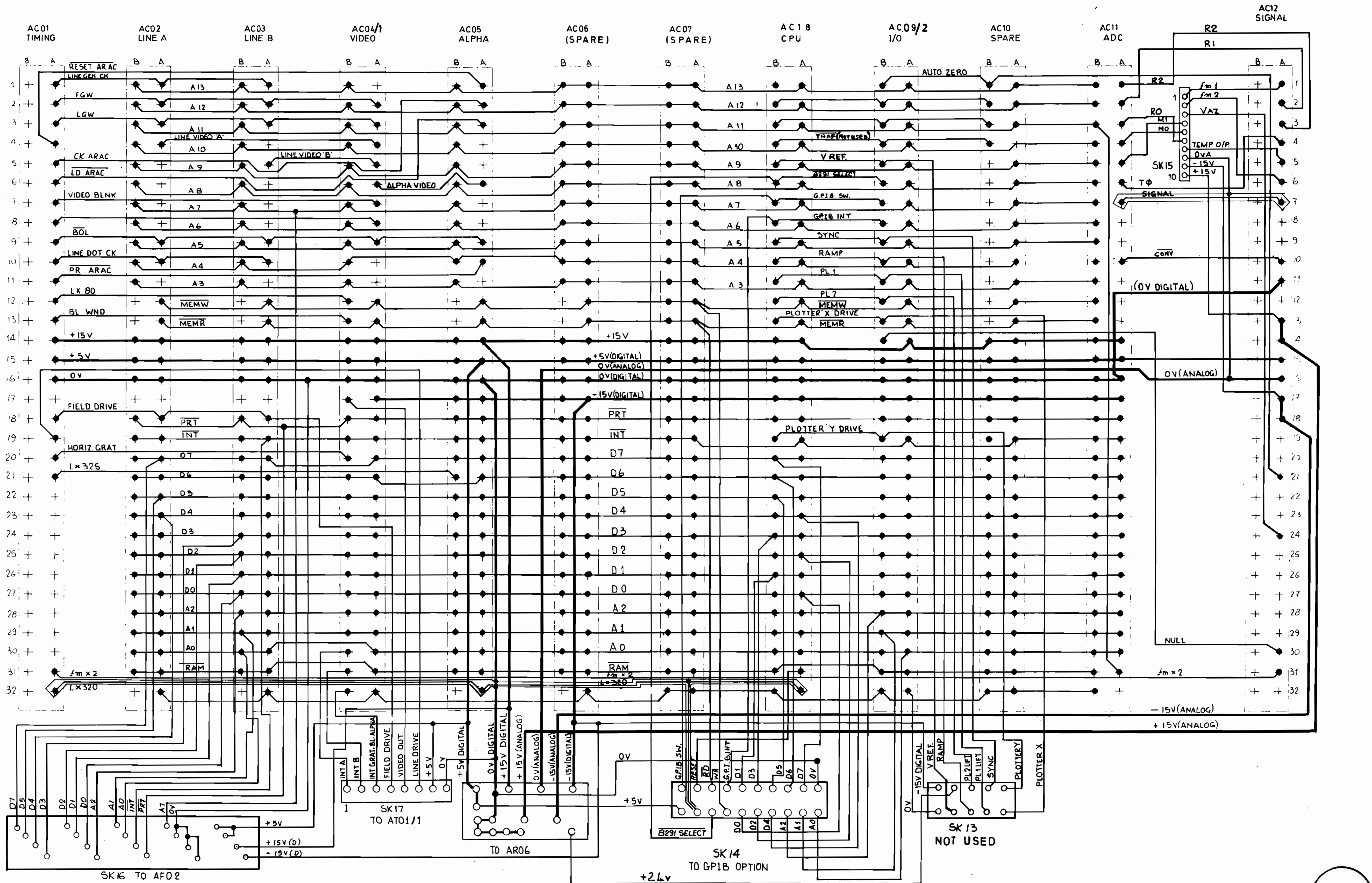
AR04/1

Fig. 15 Ramp circuit (rear panel), AR04/1



AM01

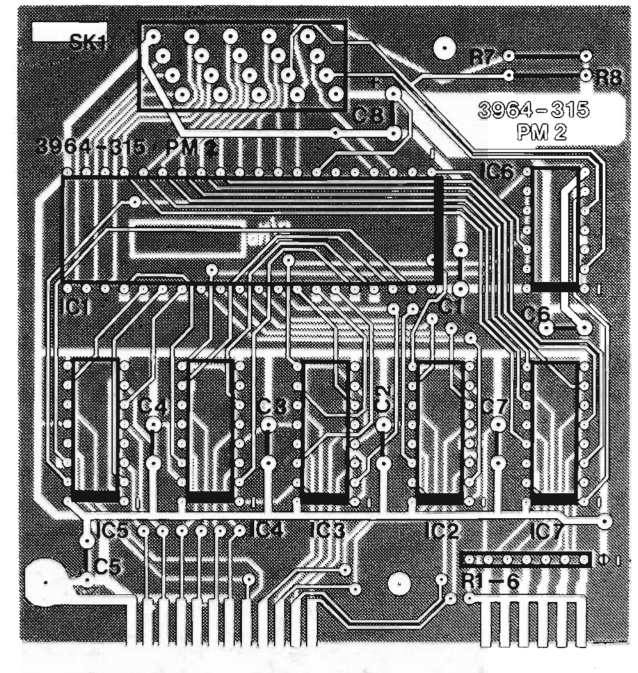
Fig. 16a Printed circuit connections, AM01

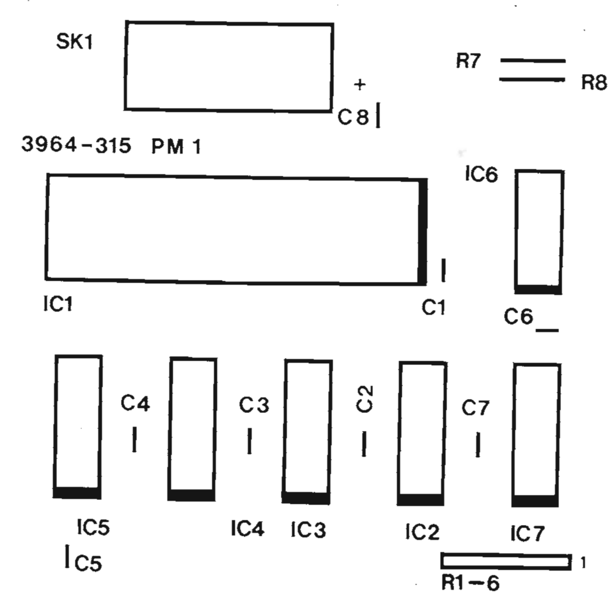


3964/920, Iss.4

AM01

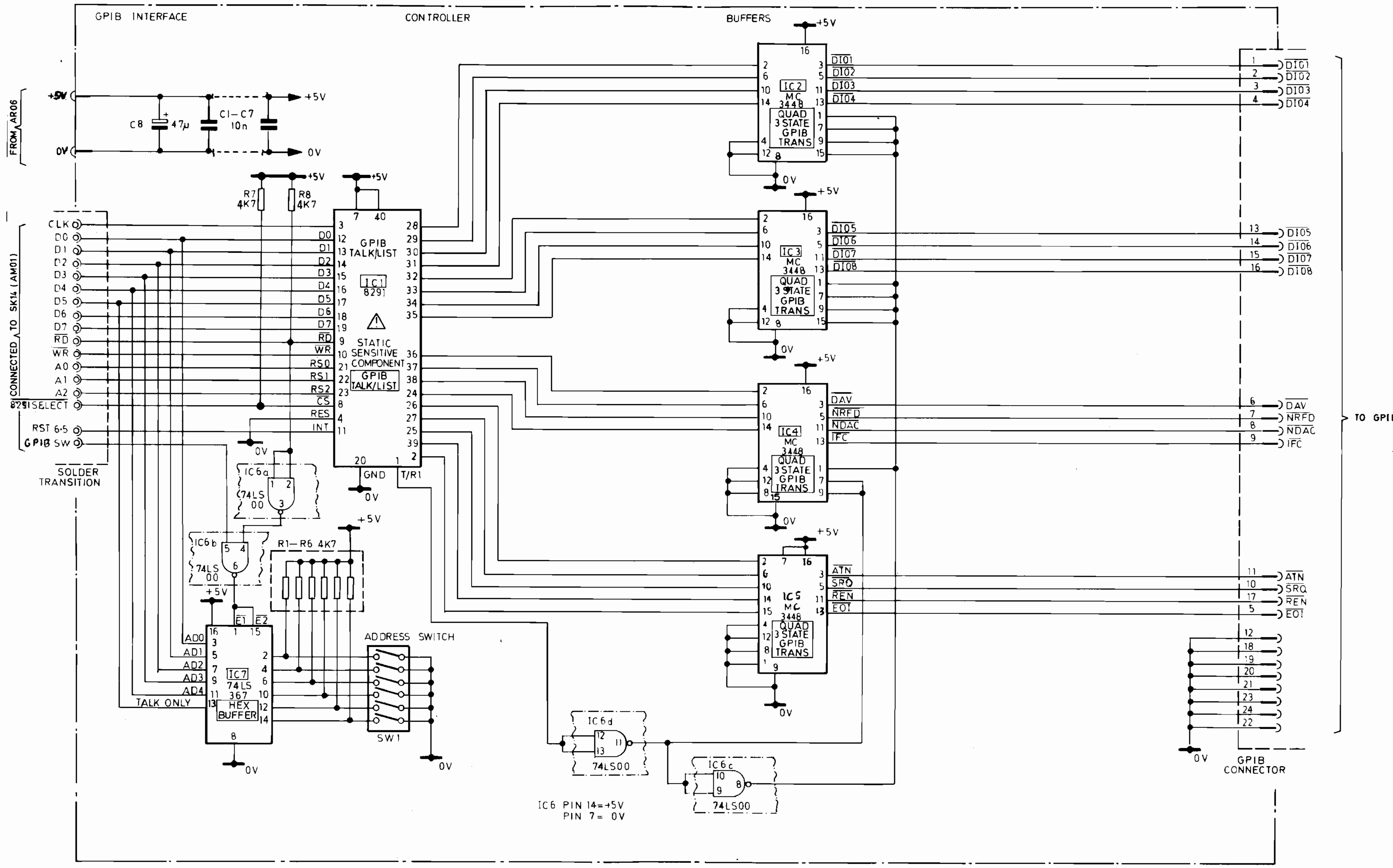
Fig. 16 Mother board, AM01





GPIB

Fig. 17a Interface component layout, GPIB



3964/921, Iss. 1

Fig. 17 Interface module, GPIB

GPIB